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APDS-9960

Digital Proximity, Ambient Light, RGB and Gesture Sensor



Data Sheet



Lead (Pb) Free
RoHS 6 fully
compliant



Description

The APDS-9960 device features advanced Gesture detection, Proximity detection, Digital Ambient Light Sense (ALS) and Color Sense (RGBC). The slim modular package, L 3.94 × W 2.36 × H 1.35 mm, incorporates an IR LED and factory calibrated LED driver for drop-in compatibility with existing footprints.

Gesture detection

Gesture detection utilizes four directional photodiodes to sense reflected IR energy (sourced by the integrated LED) to convert physical motion information (i.e. velocity, direction and distance) to a digital information. The architecture of the gesture engine features automatic activation (based on Proximity engine results), ambient light subtraction, cross-talk cancelation, dual 8-bit data converters, power saving inter-conversion delay, 32-dataset FIFO, and interrupt-driven I²C-bus communication. The gesture engine accommodates a wide range of mobile device gesturing requirements: simple UP-DOWN-RIGHT-LEFT gestures or more complex gestures can be accurately sensed. Power consumption and noise are minimized with adjustable IR LED timing.

Description continued on next page...

Applications

- Gesture Detection
- Color Sense
- Ambient Light Sensing
- Cell Phone Touch Screen Disable
- Mechanical Switch Replacement

Ordering Information

| Part Number | Packaging | Quantity |
|-------------|-------------|---------------|
| APDS-9960 | Tape & Reel | 5000 per reel |

Features

- Ambient Light and RGB Color Sensing, Proximity Sensing, and Gesture Detection in an Optical Module
- Ambient Light and RGB Color Sensing
 - UV and IR blocking filters
 - Programmable gain and integration time
 - Very high sensitivity – Ideally suited for operation behind dark glass
- Proximity Sensing
 - Trimmed to provide consistent reading
 - Ambient light rejection
 - Offset compensation
 - Programmable driver for IR LED current
 - Saturation indicator bit
- Complex Gesture Sensing
 - Four separate diodes sensitive to different directions
 - Ambient light rejection
 - Offset compensation
 - Programmable driver for IR LED current
 - 32 dataset storage FIFO
 - Interrupt driven I²C-bus communication
- I²C-bus Fast Mode Compatible Interface
 - Data Rates up to 400 kHz
 - Dedicated Interrupt Pin
- Small Package L 3.94 × W 2.36 × H 1.35 mm

Description (Cont.)

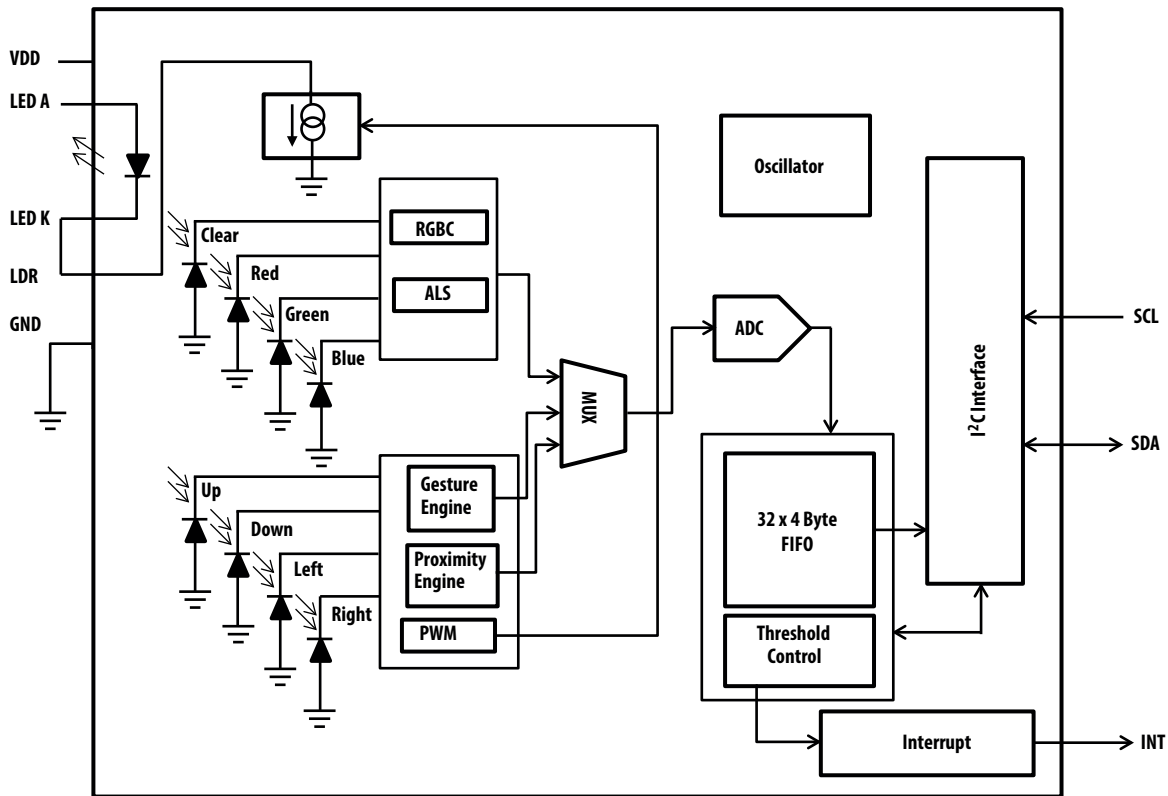
Proximity detection

The Proximity detection feature provides distance measurement (E.g. mobile device screen to user's ear) by photodiode detection of reflected IR energy (sourced by the integrated LED). Detect/release events are interrupt driven, and occur whenever proximity result crosses upper and/or lower threshold settings. The proximity engine features offset adjustment registers to compensate for system offset caused by unwanted IR energy reflections appearing at the sensor. The IR LED intensity is factory trimmed to eliminate the need for end-equipment calibration due to component variations. Proximity results are further improved by automatic ambient light subtraction.

Color and ALS detection

The Color and ALS detection feature provides red, green, blue and clear light intensity data. Each of the R, G, B, C channels have a UV and IR blocking filter and a dedicated data converter producing 16-bit data simultaneously. This architecture allows applications to accurately measure ambient light and sense color which enables devices to calculate color temperature and control display backlight.

Functional Block Diagram



I/O Pins Configuration

| Pin | Name | Type | Description |
|-----|-----------------|------|--|
| 1 | SDA | I/O | I ² C serial data I/O terminal - serial data I/O for I ² C-bus |
| 2 | INT | O | Interrupt - open drain (active low) |
| 3 | LDR | | LED driver input for proximity IR LED, constant current source LED driver |
| 4 | LEDK | | LED Cathode, connect to LDR pin when using internal LED driver circuit |
| 5 | LEDA | | LED Anode, connect to V _{LEDA} on PCB |
| 6 | GND | | Power supply ground. All voltages are referenced to GND |
| 7 | SCL | I | I ² C serial clock input terminal - clock signal for I ² C serial data |
| 8 | V _{DD} | | Power supply voltage |

Absolute Maximum Ratings over operating free-air temperature range (unless otherwise noted)*

| Parameter | Symbol | Min | Max | Units | Conditions |
|-------------------------------------|------------------|------|-----|-------|------------|
| Power supply voltage ^[1] | V _{DD} | | 3.8 | V | |
| Input voltage range | V _{IN} | -0.5 | 3.8 | V | |
| Output voltage range | V _{OUT} | -0.3 | 3.8 | V | |
| Storage temperature range | T _{stg} | -40 | 85 | °C | |

* Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 1. All voltages are with respect to GND.

Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Units |
|---|-------------------|-----|-----|-----|-------|
| Operating ambient temperature | T _A | -30 | | 85 | °C |
| Power supply voltage | V _{DD} | 2.4 | 3.0 | 3.6 | V |
| Supply voltage accuracy, V _{DD} total error including transients | | -3 | | +3 | % |
| LED supply voltage | V _{LEDA} | 3.0 | | 4.5 | V |

Operating Characteristics, V_{DD} = 3 V, T_A = 25 °C (unless otherwise noted)

| Parameter | Symbol | Min | Typ | Max | Units | Test Conditions |
|---|-------------------|------|-----|-----------------|-------|--|
| IDD supply current ^[1] | I _{DD} | | 200 | 250 | μA | Active ALS state PON = AEN = 1, PEN = 0 |
| | | | 790 | | | Proximity, LDR pulse ON, PPulse = 8 (I _{LDR} not included) |
| | | | 790 | | | Gesture, LDR pulse ON, GPulse = 8 (I _{LDR} not included) |
| | | | 38 | | | Wait state PON = 1, AEN = PEN = 0 |
| | | | 1.0 | 10.0 | | Sleep state ^[2] |
| V _{OL} INT, SDA output low voltage | V _{OL} | 0 | | 0.4 | V | 3 mA sink current |
| I _{LEAK} leakage current, SDA, SCL, INT pins | I _{LEAK} | -5 | | 5 | μA | |
| I _{LEAK} leakage current, LDR P\pin | I _{LEAK} | -10 | | 10 | μA | |
| SCL, SDA input high voltage, V _{IH} | V _{IH} | 1.26 | | V _{DD} | V | |
| SCL, SDA input low voltage, V _{IL} | V _{IL} | | | 0.54 | V | |

Notes

- Values are shown at the V_{DD} pin and do not include current through the IR LED.
- Sleep state occurs when PON = 0 and I²C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will be high.

Optical Characteristics, $V_{DD} = 3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, $\text{AGAIN} = 16\times$, $\text{AEN} = 1$ (unless otherwise noted)

| Parameter | Red Channel | | Green Channel | | Blue Channel | | Units | Test Conditions |
|-----------------------------|-------------|-----|---------------|-----|--------------|-----|-------|---------------------------------|
| | Min | Max | Min | Max | Min | Max | | |
| Irradiance responsivity [1] | 0 | 15 | 10 | 42 | 57 | 100 | % | $\lambda_D = 465\text{ nm}$ [2] |
| | 4 | 25 | 54 | 85 | 10 | 45 | | $\lambda_D = 525\text{ nm}$ [3] |
| | 64 | 120 | 0 | 14 | 3 | 29 | | $\lambda_D = 625\text{ nm}$ [4] |

Notes:

- The percentage shown represents the ratio of the respective red, green, or blue channel value to the clear channel value.
- The 465 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength $\lambda_D = 465\text{ nm}$, spectral halfwidth $\Delta\lambda_{1/2} = 22\text{ nm}$.
- The 525 nm input irradiance is supplied by an InGaN light-emitting diode with the following characteristics: dominant wavelength $\lambda_D = 525\text{ nm}$, spectral halfwidth $\Delta\lambda_{1/2} = 35\text{ nm}$.
- The 625 nm input irradiance is supplied by a AlInGaP light-emitting diode with the following characteristics: dominant wavelength $\lambda_D = 625\text{ nm}$, spectral halfwidth $\Delta\lambda_{1/2} = 15\text{ nm}$.

RGBC Characteristics, $V_{DD} = 3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, $\text{AGAIN} = 16\times$, $\text{AEN} = 1$ (unless otherwise noted)

| Parameter | Min | Typ | Max | Units | Test Conditions |
|--|-------|-------|-------|-------------------------------------|--|
| Dark ALS count value | | 0 | 3 | counts | $E_e = 0$, $\text{AGAIN} = 64\times$, $\text{ATIME} = 0\times\text{DB}$ (100 ms) |
| ADC integration time step size | | 2.78 | | ms | $\text{ATIME} = 0\times\text{FF}$ |
| ADC number of integration steps | 1 | | 256 | steps | |
| Full scale ADC counts per step | | | 1025 | counts | |
| Full scale ADC count value | | | 65535 | counts | $\text{ATIME} = 0\times\text{C0}$ (175 ms) |
| Gain scaling, relative to $1\times$ gain setting | 3.6 | 4 | 4.4 | | $4\times$ |
| | 14.4 | 16 | 17.6 | | $16\times$ |
| | 57.6 | 64 | 70.4 | | $64\times$ |
| Clear channel irradiance responsivity | 18.88 | 23.60 | 28.32 | counts/ $(\mu\text{W}/\text{cm}^2)$ | Neutral white LED, $\lambda = 560\text{ nm}$ |

Proximity Characteristics, $V_{DD} = 3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, $\text{PEN} = 1$ (unless otherwise noted)

| Parameter | Min | Typ | Max | Units | Test Conditions |
|--|-----|-------|-----|---------------|--|
| ADC conversion time step size | | 696.6 | | μs | |
| ADC number of integration steps | | 1 | | steps | |
| Full scale ADC counts | | | 255 | counts | |
| LED pulse count [1] | 1 | | 64 | pulses | |
| LED pulse width – LED on time [2] | | 4 | | μs | $\text{PPLEN} = 0$ |
| | | 8 | | | $\text{PPLEN} = 1$ |
| | | 16 | | | $\text{PPLEN} = 2$ |
| | | 32 | | | $\text{PPLEN} = 3$ |
| LED drive current [3] | | 100 | | mA | $\text{LDRIVE} = 0$ |
| | | 50 | | | $\text{LDRIVE} = 1$ |
| | | 25 | | | $\text{LDRIVE} = 2$ |
| | | 12.5 | | | $\text{LDRIVE} = 3$ |
| LED boost [3] | | 100 | | % | $\text{LED_BOOST} = 0$ |
| | | 150 | | | $\text{LED_BOOST} = 1$ |
| | | 200 | | | $\text{LED_BOOST} = 2$ |
| | | 300 | | | $\text{LED_BOOST} = 3$ |
| Proximity ADC count value, no object [4] | | 10 | 25 | counts | $V_{\text{LEDA}} = 3\text{ V}$, $\text{LDRIVE} = 100\text{ mA}$, $\text{PPULSE} = 8$, $\text{PGAIN} = 4\times$, $\text{PPLEN} = 8\text{ } \mu\text{s}$, $\text{LED_BOOST} = 100\%$, open view (no glass) and no reflective object above the module. |

Table continued on next page...

Proximity Characteristics, $V_{DD} = 3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, PEN = 1 (unless otherwise noted) (continued)

| Parameter | Min | Typ | Max | Units | Test Conditions |
|--|-----|-----|-----|--------|---|
| Proximity ADC count value, 100 mm distance object [5, 6] | 96 | 120 | 144 | counts | Reflecting object – 73 mm × 83 mm Kodak 90% grey card, 100 mm distance, $V_{LEDA} = 3\text{ V}$, $LDRIVE = 100\text{ mA}$, $PPULSE = 8$, $PGAIN = 4x$, $PPLEN = 8\text{ }\mu\text{s}$, $LED_BOOST = 100\%$, open view (no glass) above the module. |

Notes:

1. This parameter is ensured by design and characterization and is not 100% tested. 8 pulses are the recommended driving conditions. For other driving conditions, contact Avago Field Sales.
2. Value may be as much as 1.36 μs longer than specified.
3. Value is factory-adjusted to meet the Proximity count specification. Considerable variation (relative to the typical value) is possible after adjustment. LED BOOST increases current setting (as defined by LDRIVE or GLDRIVE). For example, if LDRIVE = 0 and LED BOOST = 100%, LDR current is 100 mA.
4. Proximity offset value varies with power supply characteristics and noise.
5. ILEDA is factory calibrated to achieve this specification. Offset and crosstalk directly sum with this value and is system dependent.
6. No glass or aperture above the module. Tested value is the average of 5 consecutive readings.

Gesture Characteristics, $V_{DD} = 3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, GEN = 1 (unless otherwise noted)

| Parameter | Min | Typ | Max | Units | Test Conditions |
|--|-----|------|-----|---------------|--|
| ADC conversion time step size [1] | | 1.39 | | ms | |
| LED pulse count [2] | 1 | | 64 | pulses | |
| LED pulse width – LED on time [3] | | 4 | | μs | $GPLEN = 0$ |
| | | 8 | | | $GPLEN = 1$ |
| | | 12 | | | $GPLEN = 2$ |
| | | 16 | | | $GPLEN = 3$ |
| LED drive current [4] | | 100 | | mA | $GLDRIVE = 0$ |
| | | 50 | | | $GLDRIVE = 1$ |
| | | 25 | | | $GLDRIVE = 2$ |
| | | 12.5 | | | $GLDRIVE = 3$ |
| LED boost [4] | | 100 | | % | $LED_BOOST = 0$ |
| | | 150 | | | $LED_BOOST = 1$ |
| | | 200 | | | $LED_BOOST = 2$ [5] |
| | | 300 | | | $LED_BOOST = 3$ [5] |
| Gesture ADC count value, no object [6] | | 10 | 25 | counts | $V_{LEDA} = 3\text{ V}$, $GLDRIVE = 100\text{ mA}$, $GPULSE = 8$, $GGAIN = 4x$, $GPLEN = 8\text{ }\mu\text{s}$, $LED_BOOST = 100\%$, open view (no glass) and no reflective object above the module, sum of UP & DOWN photodiodes. |
| Gesture ADC count value [7, 8] | 96 | 120 | 144 | counts | Reflecting object – 73 mm × 83 mm Kodak 90% grey card, 100 mm distance, $V_{LEDA} = 3\text{ V}$, $GLDRIVE = 100\text{ mA}$, $GPULSE = 8$, $GGAIN = 4x$, $GPLEN = 8\text{ }\mu\text{s}$, $LED_BOOST = 100\%$, open view (no glass) above the module, sum of UP & DOWN photodiodes. |
| Gesture wait step size | | 2.78 | | ms | $GTIME = 0x01$ |

Notes:

1. Each U/D or R/L pair requires a conversion time of 696.6 μs . For all four directions the conversion requires twice as much time.
2. This parameter ensured by design and characterization and is not 100% tested. 8 pulses are the recommended driving conditions. For other driving conditions, contact Avago Field Sales.
3. Value may be as much as 1.36 μs longer than specified.
4. Value is factory-adjusted to meet the Gesture count specification. Considerable variation (relative to the typical value) is possible after adjustment.
5. When operating at these LED drive conditions, it is recommended to separate the VDD and VLEDA supplies.
6. Gesture offset value varies with power supply characteristics and noise.
7. ILEDA is factory calibrated to achieve this specification. Offset and crosstalk directly sum with this value and is system dependent.
8. No glass or aperture above the module. Tested value is the average of 5 consecutive readings.

IR LED Characteristics, $V_{DD} = 3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$ (unless otherwise noted)

| Parameter | Min | Typ | Max | Units | Test Conditions |
|---|-----|-----|-----|-------|-----------------------|
| Peak Wavelength, λ_p | | 950 | | nm | $I_F = 20\text{ mA}$ |
| Spectrum Width, Half Power, $\Delta\lambda$ | | 30 | | nm | $I_F = 20\text{ mA}$ |
| Optical Rise Time, T_R | | 20 | | ns | $I_F = 100\text{ mA}$ |
| Optical Fall Time, T_F | | 20 | | ns | $I_F = 100\text{ mA}$ |

Wait Characteristics, $V_{DD} = 3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, $WEN = 1$ (unless otherwise noted)

| Parameter | Min | Typ | Max | Units | Test Conditions |
|----------------|-----|------|-----|-------|-----------------|
| Wait Step Size | | 2.78 | | ms | WTIME = 0xFF |

AC Electrical Characteristics, $V_{DD} = 3\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$ (unless otherwise noted) *

| Parameter | Symbol | Min. | Max. | Unit |
|---|--------------|------|------|---------------|
| Clock frequency (I ² C-bus only) | f_{SCL} | 0 | 400 | kHz |
| Bus free time between a STOP and START condition | t_{BUF} | 1.3 | – | μs |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated | $t_{HD,STA}$ | 0.6 | – | μs |
| Set-up time for a repeated START condition | $t_{SU,STA}$ | 0.6 | – | μs |
| Set-up time for STOP condition | $t_{SU,STO}$ | 0.6 | – | μs |
| Data hold time | $t_{HD,DAT}$ | 30 | – | ns |
| Data set-up time | $t_{SU,DAT}$ | 100 | – | ns |
| LOW period of the SCL clock | t_{LOW} | 1.3 | – | μs |
| HIGH period of the SCL clock | t_{HIGH} | 0.6 | – | μs |
| Clock/data fall time | t_f | 20 | 300 | ns |
| Clock/data rise time | t_r | 20 | 300 | ns |
| Input pin capacitance | C_i | – | 10 | pF |

* Specified by design and characterization; not production tested.

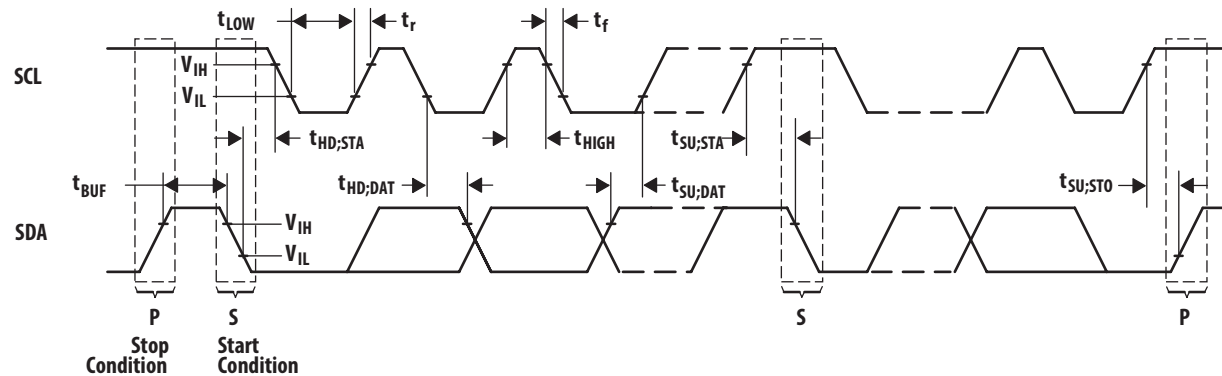


Figure 1. Timing Diagrams

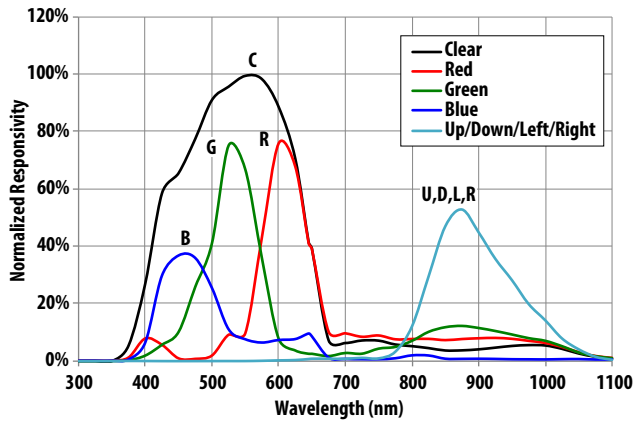


Figure 2. Spectral Response

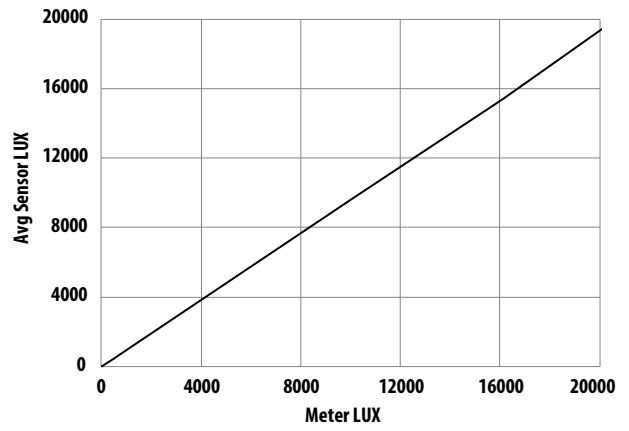


Figure 3a. ALS Sensor LUX vs Meter LUX using White Light

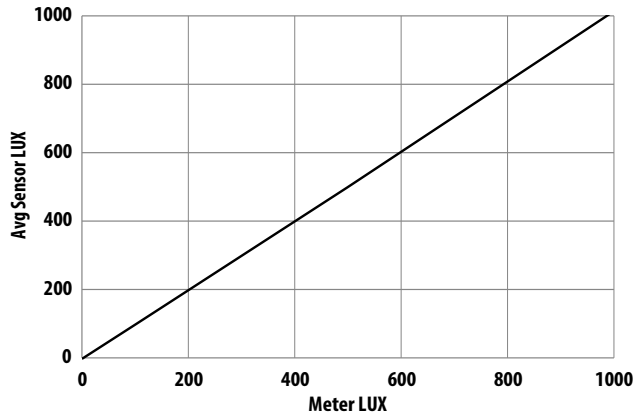


Figure 3b. ALS Sensor LUX vs Meter LUX using Incandescent Light

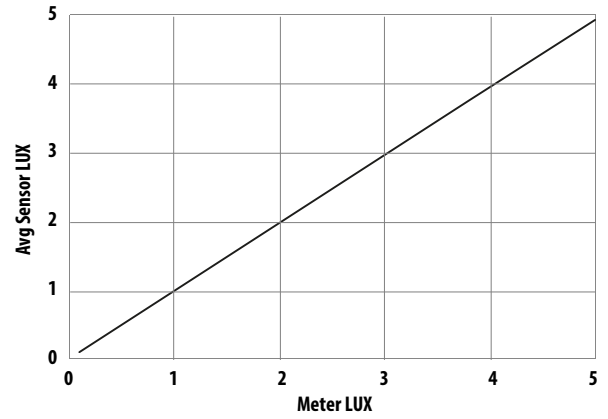


Figure 3c. ALS Sensor LUX vs Meter LUX using White Light

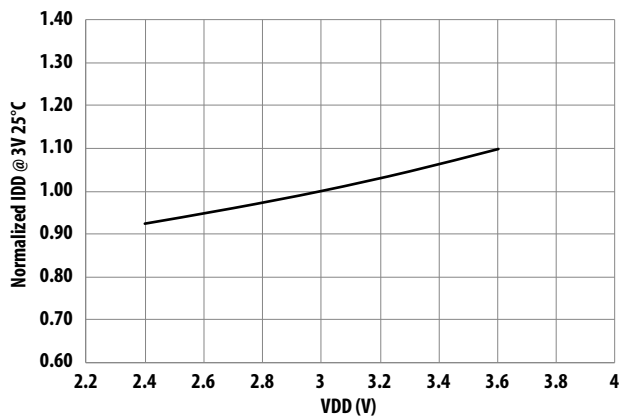


Figure 4a. Normalized IDD vs. VDD

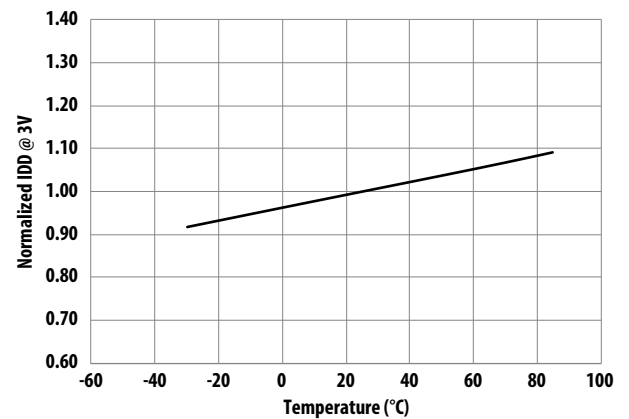


Figure 4b. Normalized IDD vs. Temperature

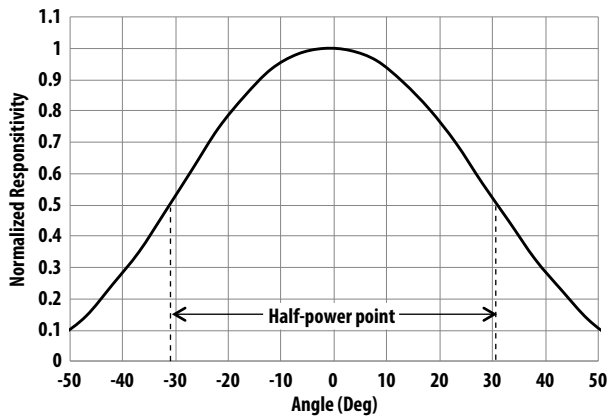


Figure 5a. Normalized PD Responsivity vs. Angular Displacement

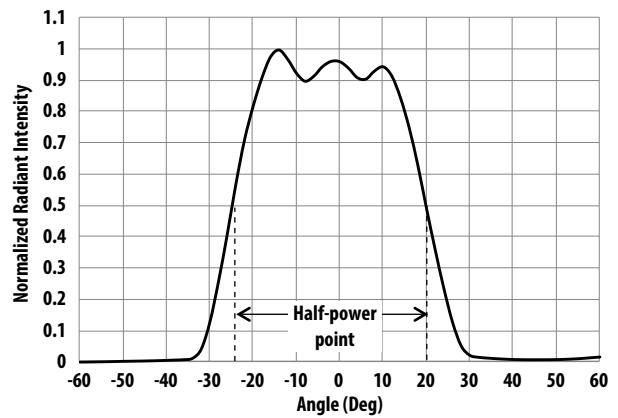


Figure 5b. Normalized LED Angular Emitting Profile

I²C-bus Protocol

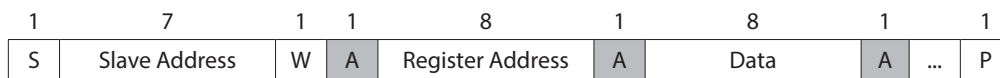
Interface and control are accomplished through an I²C-bus serial compatible interface (standard or fast mode) to a set of registers that provide access to device control functions and output data. The devices support the 7-bit I²C-bus addressing protocol.

The device supports a single slave address of 0x39 Hex using 7-bit addressing protocol. (Contact factory for other addressing options.)

- A Acknowledge (0)
- N Not Acknowledged (1)
- P Stop Condition
- R Read (1)
- S Start Condition
- Sr Repeated Start Condition
- W Write (0)
- ... Continuation of protocol
- Master-to-Slave
- Slave-to-Master

The I²C-bus standard provides for three types of bus transaction: read, write, and a combined protocol. During a write operation, the first byte written is a command byte followed by data. In a combined protocol, the first byte written is the command byte followed by reading a series of bytes. If a read command is issued, the register address from the previous command will be used for data access. Likewise, if the MSB of the command is not set, the device will write a series of bytes at the address stored in the last valid command with a register address. The command byte contains either control information or a 5-bit register address. The control commands can also be used to clear interrupts.

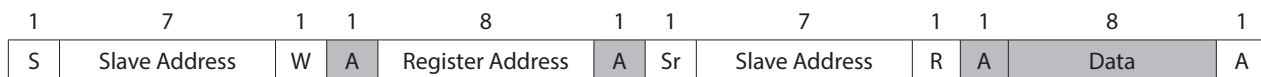
The I²C-bus protocol was developed by Philips (now NXP). For a complete description of the I²C-bus protocol, please review the NXP I²C-bus design specification at <http://www.i2c-bus.org/references/>.



I²C-bus Write Protocol



I²C-bus Read Protocol



I²C-bus Read Protocol - Combined Format

I²C-bus Protocol

Detailed Description

Gesture detection, proximity detection, and RGBC color sense/ambient light sense functionality is controlled by a state machine, as depicted in Figure 6, which reconfigures on-chip analog resources when each functional engine is entered. Functional states/engines can be individually included or excluded from the progression of state machine flow. Each functional engine contains controls (E.g., Gain, ADC integration time, wait time, persistence, thresholds, etc.) that govern operation. Control of the Led Drive pin, LDR, is shared between Proximity and Gesture functionality. The color/ALS engine does not use the IR LED, but cross talk from IR LED emissions during an optical pattern transmission may affect results.

The operational cycle of the device for Gesture/Proximity/Color is as depicted in Figure 6 and Figure 7.

Upon power-up, POR, the device initializes and immediately enters the low power SLEEP state. In this operational state the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If I²C transaction occurs during this state, the oscillator and I²C core wakeup temporarily to service the communication. Once the Power ON bit, PON, is enabled, the internal oscillator and attendant circuitry are active, but power consumption remains low until one of the functional engine blocks are entered. The first time the SLEEP state is exited and any of the analog engines are enabled (PEN, GEN, AEN

=1) an EXIT SLEEP pause occurs; followed by an immediate entry into the selected engine. If multiple engines are enabled, then the operational flow progresses in the following order: idle, proximity, gesture (if GMODE = 1), wait, color/ALS, and sleep (if SAI = 1 and INT pin is asserted). The wait operational state functions to reduce the power consumption and data collection rate. If wait is enabled, WEN=1, the delay is adjustable from 2.78 ms to 8.54 s, as set by the value in the WTIME register and WLONG control bit.

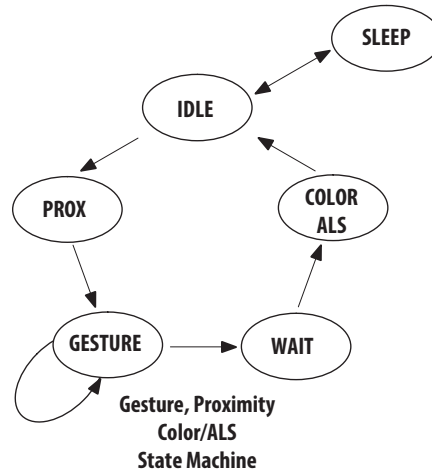


Figure 6. Simplified State Diagram

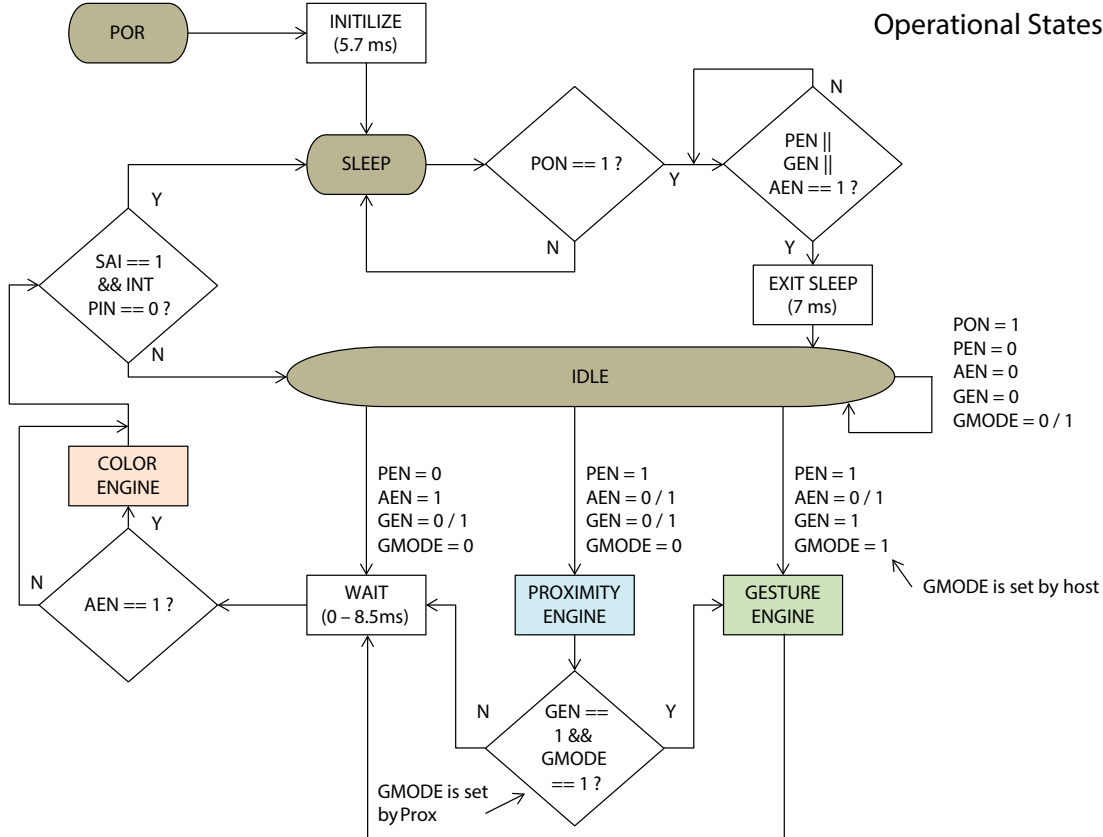


Figure 7. Detailed State Diagram

Sleep After Interrupt Operation

After all the enabled engines/operational states have executed, causing a hardware interrupt, the state machine returns to either IDLE or SLEEP, as selected by the Sleep After Interrupt bit, SAI. SLEEP is entered when two conditions are met: SAI = 1, and the INT pin has been asserted. Entering SLEEP does not automatically change any of the register settings (E.g. PON bit is still high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated by an I²C clear of the INT pin or if SAI bit is cleared.

Proximity Operation

The Proximity detection feature provides distance measurement by photodiode detection of reflected IR energy sourced by the integrated LED. The following registers and control bits govern proximity operation and the operational flow is depicted in Figure 8.

Table 1. Proximity Controls

| Register/Bit | Address | Description |
|-------------------|-----------|---------------------------------------|
| ENABLE<PON> | 0x80<0> | Power ON |
| ENABLE<PEN> | 0x80<2> | Proximity Enable |
| ENABLE<PIEN> | 0x80<5> | Proximity Interrupt Enable |
| PILT | 0x89 | Proximity low threshold |
| PIHT | 0x8B | Proximity high threshold |
| PERS<PPERS> | 0x8C<7:4> | Proximity Interrupt Persistence |
| PPULSE<PPLEN> | 0x8E<7:6> | Proximity Pulse Length |
| PPULSE<PPULSE> | 0x8E<5:0> | Proximity Pulse Count |
| CONTROL<PGAIN> | 0x8F<3:2> | Proximity Gain Control |
| CONTROL<LDRIVE> | 0x8F<7:6> | LED Drive Strength |
| CONFIG2<PSIEN> | 0x90<7> | Proximity Saturation Interrupt Enable |
| CONFIG2<LEDBOOST> | 0x90<5:4> | Proximity/Gesture LED Boost |
| STATUS<PGSAT> | 0x93<6> | Proximity Saturation |
| STATUS<PINT> | 0x93<5> | Proximity Interrupt |
| STATUS<PVALID> | 0x93<1> | Proximity Valid |
| PDATA | 0x9C | Proximity Data |
| POFFSET_UR | 0x9D | Proximity Offset UP/RIGHT |
| POFFSET_DL | 0x9E | Proximity Offset DOWN/LEFT |
| CONFIG3<PCMP> | 0x9F<5> | Proximity Gain Compensation Enable |
| CONFIG3<PMSK_U> | 0x9F<3> | Proximity Mask UP Enable |
| CONFIG3<PMSK_D> | 0x9F<2> | Proximity Mask DOWN Enable |
| CONFIG3<PMSK_L> | 0x9F<1> | Proximity Mask LEFT Enable |
| CONFIG3<PMSK_R> | 0x9F<0> | Proximity Mask RIGHT Enable |
| PICLEAR | 0xE5 | Proximity Interrupt Clear |
| AICLEAR | 0xE7 | All Non-Gesture Interrupt Clear |

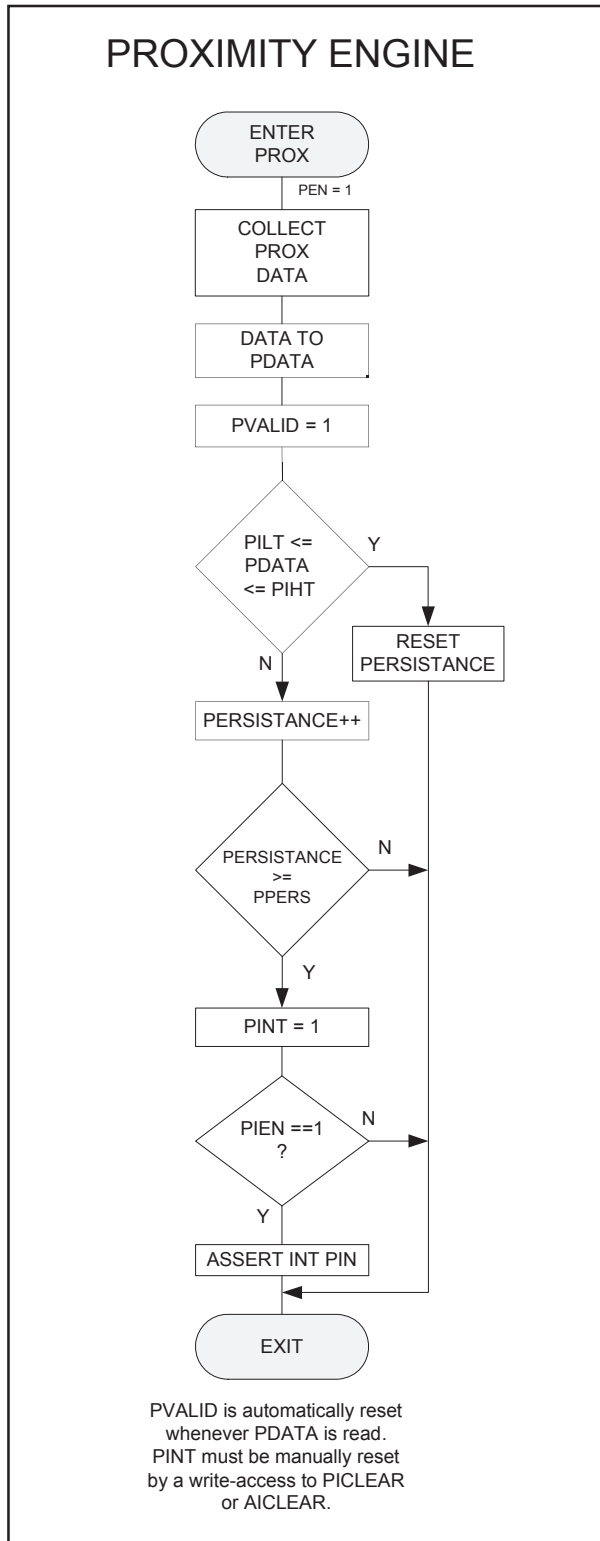


Figure 8. Detailed Proximity Diagram

Proximity results are affected by three fundamental factors: IR LED emission, IR reception, and environmental factors, including target distance and surface reflectivity.

The IR reception signal path begins with IR detection from four [directional gesture] photodiodes and ends with the 8-bit proximity result in PDATA register. Signal from the photodiodes is combined, amplified, and offset adjusted to optimize performance. The same four photodiodes are used for gesture operation as well as proximity operation. Diodes are paired to form two signal paths: UP/RIGHT and DOWN/LEFT. Regardless of pairing, any of the photodiodes can be masked to exclude its contribution to the proximity result. Masking one of the paired diodes effectively reduces the signal by half and causes the full-scale result to be reduced from 255 to 127. To correct this reduction in full-scale, the proximity gain compensation bit, PCMP, can be set, returning F.S. to 255. Gain is adjustable from 1x to 8x using the PGAIN control bits. Offset correction or cross-talk compensation is accomplished by adjustment to the POFFSET_UR and POFSET_DL registers. The analog circuitry of the device applies the offset value as a subtraction to the signal accumulation; therefore a positive offset value has the effect of decreasing the results.

Optically, the IR emission appears as a pulse train. The number of pulses is set by the PPULSE bits and the period of each pulse is adjustable using the PPLEN bits. The intensity of the IR emission is selectable using the LDRIVE control bits; corresponding to four, factory calibrated, current levels. If a higher intensity is required (E.g. longer detection distance or device placement beneath dark glass) then the LEDBOOST bit can be used to boost current up to an additional 300%.

LED duty cycle and subsequent power consumption of the integrated IR LED can be calculated using the following table shown in Table 2, and equations. If proximity events are separated by a wait time, as set by AWAIT and WLONG, then the total LED off time must be increased by the wait time.

Table 2. Approximate Proximity Timing

| PPLEN | t _{INIT} (μs) | t _{LED ON} (μs) | t _{ACC} (μs) | t _{CNVT} (μs) |
|-------|---------------------------|-----------------------------|--------------------------|---------------------------|
| 4 μs | 40.8 | 5.4 | 28.6 | 796.6 |
| 8 μs | 44.9 | 9.5 | 36.73 | 796.6 |
| 16 μs | 53.0 | 17.7 | 53.1 | 796.6 |
| 32 μs | 69.4 | 34.0 | 85.7 | 796.6 |

$$t_{\text{PROX RESULT}} = t_{\text{INIT}} + t_{\text{CNVT}} + \text{PPULSE} \times t_{\text{ACC}}$$

$$t_{\text{TOTAL LED ON}} = \text{PPULSE} \times t_{\text{LED ON}}$$

$$t_{\text{TOTAL LED OFF}} = t_{\text{PROX RESULT}} - t_{\text{TOTAL LED ON}}$$

An Interrupt can be generated with each new proximity result or whenever proximity results exceed or fall below levels set in the PIHT and/or PILT threshold registers. To prevent premature/ false interrupts an interrupt persistence filter is also included; interrupts will only be asserted if the consecutive number of out-of-threshold results is equal or greater than the value set by PPERS. Each “in-threshold” proximity result, PDATA, will reset the persistence count. If the analog circuitry becomes saturated, the PGSAT bit will be asserted to indicate PDATA results

may not be accurate. The PINT and PGSAT bits are always available for I²C polling, but PIEN bit must be set for PINT to assert a hardware interrupt on the INT pin. Similarly, saturation of the analog data converter can be detected by polling PGSAT bit; to enable this feature the PSIEN bit must be set. PVALID is cleared by reading PDATA. PGSAT, and PINT are cleared by “address accessing” (i.e. I²C transaction consisting of only two bytes: chip address, followed by a register address with R/W=1) PICLEAR or AICLEAR.

Table 3. Color / ALS Controls

| Register/Bit | Address | Description |
|-----------------|-----------|---|
| ENABLE<PON> | 0x80<0> | Power ON |
| ENABLE<AEN> | 0x80<1> | ALS Enable |
| ENABLE<AIEN> | 0x80<4> | ALS Interrupt Enable |
| ENABLE<WEN> | 0x80<3> | Wait Enable |
| ATIME | 0x81 | ALS ADC Integration Time |
| WTIME | 0x83 | Wait Time |
| AILTL | 0x84 | ALS low threshold, lower byte |
| AILTH | 0x85 | ALS low threshold, upper byte |
| AIHTL | 0x86 | ALS high threshold, lower byte |
| AIHTH | 0x87 | ALS high threshold, upper byte |
| PERS<APERS> | 0x8C<3:0> | ALS Interrupt Persistence |
| CONFIG1<WLONG> | 0x8D<1> | Wait Long Enable |
| CONTROL<AGAIN> | 0x8F<1:0> | ALS Gain Control |
| CONFIG2<CPSIEN> | 0x90<6> | Clear diode Saturation Interrupt Enable |
| STATUS<CPSAT> | 0x93<7> | Clear Diode Saturation |
| STATUS<AINT> | 0x93<4> | ALS Interrupt |
| STATUS<AVALID> | 0x93<0> | ALS Valid |
| CDATAL | 0x94 | Clear Data, Low byte |
| CDATAH | 0x95 | Clear Data, High byte |
| RDATA L | 0x96 | Red Data, Low byte |
| RDATAH | 0x97 | Red Data, High byte |
| GDATA L | 0x98 | Green Data, Low byte |
| GDATAH | 0x99 | Green Data, High byte |
| BDATA L | 0x9A | Blue Data, Low byte |
| BDATAH | 0x9B | Blue Data, High byte |
| CICLEAR | 0xE5 | Clear Channel Interrupt Clear |
| AICLEAR | 0xE7 | All Non-Gesture Interrupt Clear |

Color and Ambient Light Sense Operation

The Color and Ambient Light Sense detection functionality uses an array of color and IR filtered photodiodes to measure red, green, and blue content of light, as well as the non-color filtered clear channel. The following registers and control bits govern Color/ALS operation and the operational flow is depicted in Figure 9.

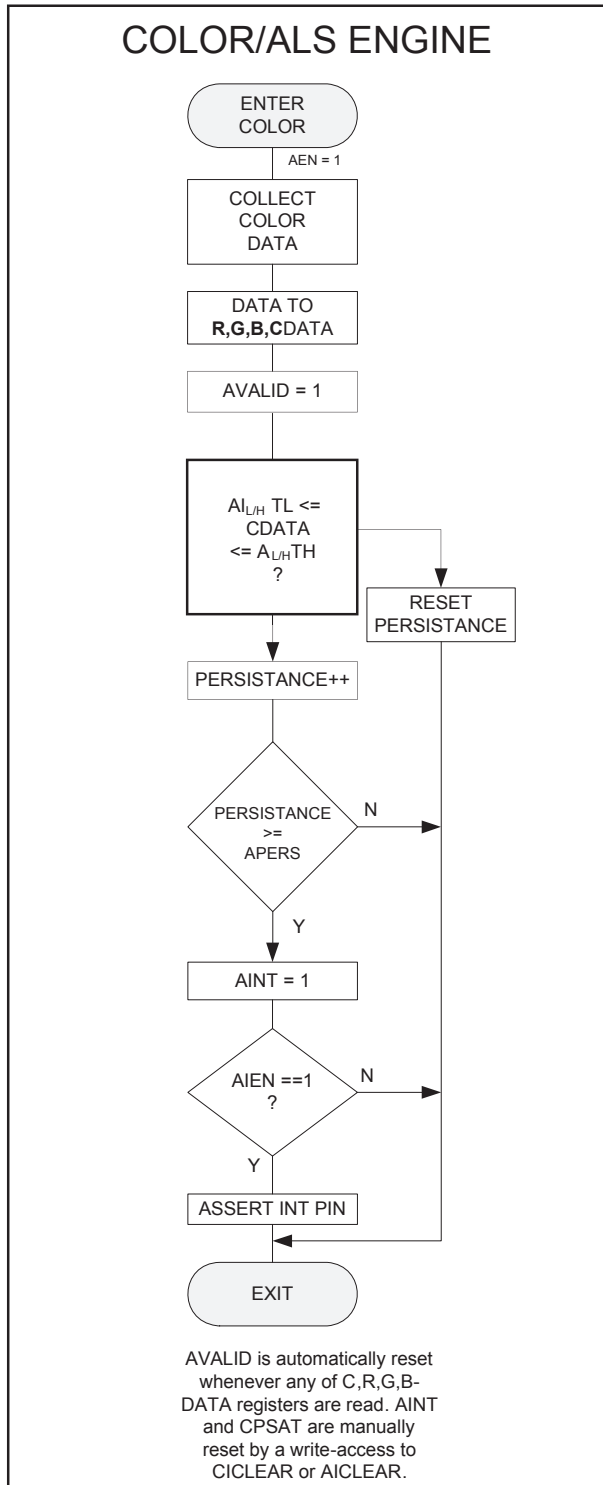


Figure 9. Color / ALS State Diagram

The Color/ALS reception signal path begins with filtered RGBC detection at the photodiodes and ends with the 16-bit results in the RGBC data registers. Signal from the photodiode array accumulates for a period of time set by the value in ATIME before the results are placed into the RGBCDATA registers. Gain is adjustable from 1x to 64x, and is determined by the setting of CONTROL<AGAIN>. Performance characteristics such as accuracy, resolution, conversion speed, and power consumption can be adjusted to meet the needs of the application.

Before entering (re-entering) the Color/ALS engine, an adjustable, low power consumption, delay is entered. The wait time for this delay is selectable using the WEN, WTIME and WLONG control bits and ranges from 0 to 8.54s. During this period the internal oscillator is still running, but all other circuitry is deactivated.

An interrupt can be generated whenever Clear Channel results exceed or fall below levels set in the AILT/AIHTL and/or AILTH/AIHTH threshold registers. To prevent premature/false interrupts a persistence filter is also included; interrupts will only be asserted if the consecutive number of out-of-threshold results is equal or greater than the value set by APERS. Each "in-threshold" Clear channel result, CDATA, will reset the persistence count. If the analog circuitry becomes saturated, the ASAT bit will be asserted to indicate RGBCDATA results may not be accurate. The AINT and CPSAT bits are always available for I²C polling, but AIEN bit must be set for AINT to assert a hardware interrupt on the INT pin. Similarly, saturation of the analog data converter can be detected by polling CPSAT bit; to enable this feature the CPSIEN bit must be set. AVALID is cleared by reading RGBCDATA. ASAT, and AINT are cleared by "address accessing" (i.e. I²C transaction consisting of only two bytes: chip address, followed by a register address with R/W=1) CICLEAR or AICLEAR. RGBC results can be used to calculate ambient light levels (i.e. Lux) and color temperature (i.e. Kelvin).

Gesture Operation

The Gesture detection feature provides motion detection by utilizing directionally sensitive photodiodes to sense reflected IR energy sourced by the integrated LED. The following registers and control bits govern gesture operation and the operational flow is depicted in Figure 10.

Table 4. Gesture Controls

| Register/Bit | Address | Description |
|---------------------|-----------|-----------------------------------|
| ENABLE<PON> | 0x80<0> | Power ON |
| ENABLE<GEN> | 0x80<6> | Gesture Enable |
| GPENTH | 0xA0 | Gesture Proximity Entry Threshold |
| GEXTH | 0xA1 | Gesture Exit Threshold |
| GCONFIG1<GFIFOTH> | 0xA2<7:6> | Gesture FIFO Threshold |
| GCONFIG1<GEXMSK> | 0xA2<5:2> | Gesture Exit Mask |
| GCONFIG1<GEXPERS> | 0xA2<1:0> | Gesture Exit Persistence |
| GCONFIG2<GGAIN> | 0xA3<6:5> | Gesture Gain Control |
| GCONFIG2<GLDRIVE> | 0xA3<4:3> | Gesture LED Drive Strength |
| GCONFIG2<GWTIME> | 0xA3<2:0> | Gesture Wait Time |
| STATUS<PGSAT> | 0x93<6> | Gesture Saturation |
| CONFIG2<LEDBOOST> | 0x90<5:4> | Gesture/Proximity LED Boost |
| GOFFSET_U | 0xA4 | Gesture Offset, UP |
| GOFFSET_D | 0xA5 | Gesture Offset, DOWN |
| GOFFSET_L | 0xA7 | Gesture Offset, LEFT |
| GOFFSET_R | 0xA9 | Gesture Offset, RIGHT |
| GPULSE<GPULSE> | 0xA6<5:0> | Pulse Count |
| GPULSE<GPLEN> | 0xA6<7:6> | Gesture Pulse Length |
| GCONFIG3<GDIMS> | 0xAA<1:0> | Gesture Dimension Select |
| GCONFIG4<GFIFO_CLR> | 0xAB<2> | Gesture FIFO Clear |
| GCONFIG4<GIEN> | 0xAB<1> | Gesture Interrupt Enable |
| GCONFIG4<GMODE> | 0xAB<0> | Gesture Mode |
| GFLVL | 0xAE | Gesture FIFO Level |
| GSTATUS<GFOV> | 0xAF<1> | Gesture FIFO Overflow |
| GSTATUS<GVALID> | 0xAF<0> | Gesture Valid |
| GFIFO_U | 0xFC | Gesture FIFO Data, UP |
| GFIFO_D | 0xFD | Gesture FIFO Data, DOWN |
| GFIFO_L | 0xFE | Gesture FIFO Data, LEFT |
| GFIFO_R | 0xFF | Gesture FIFO Data, RIGHT |
| CONFIG1<LOWPOW> | 0x8D | Low Power Clock Mode |

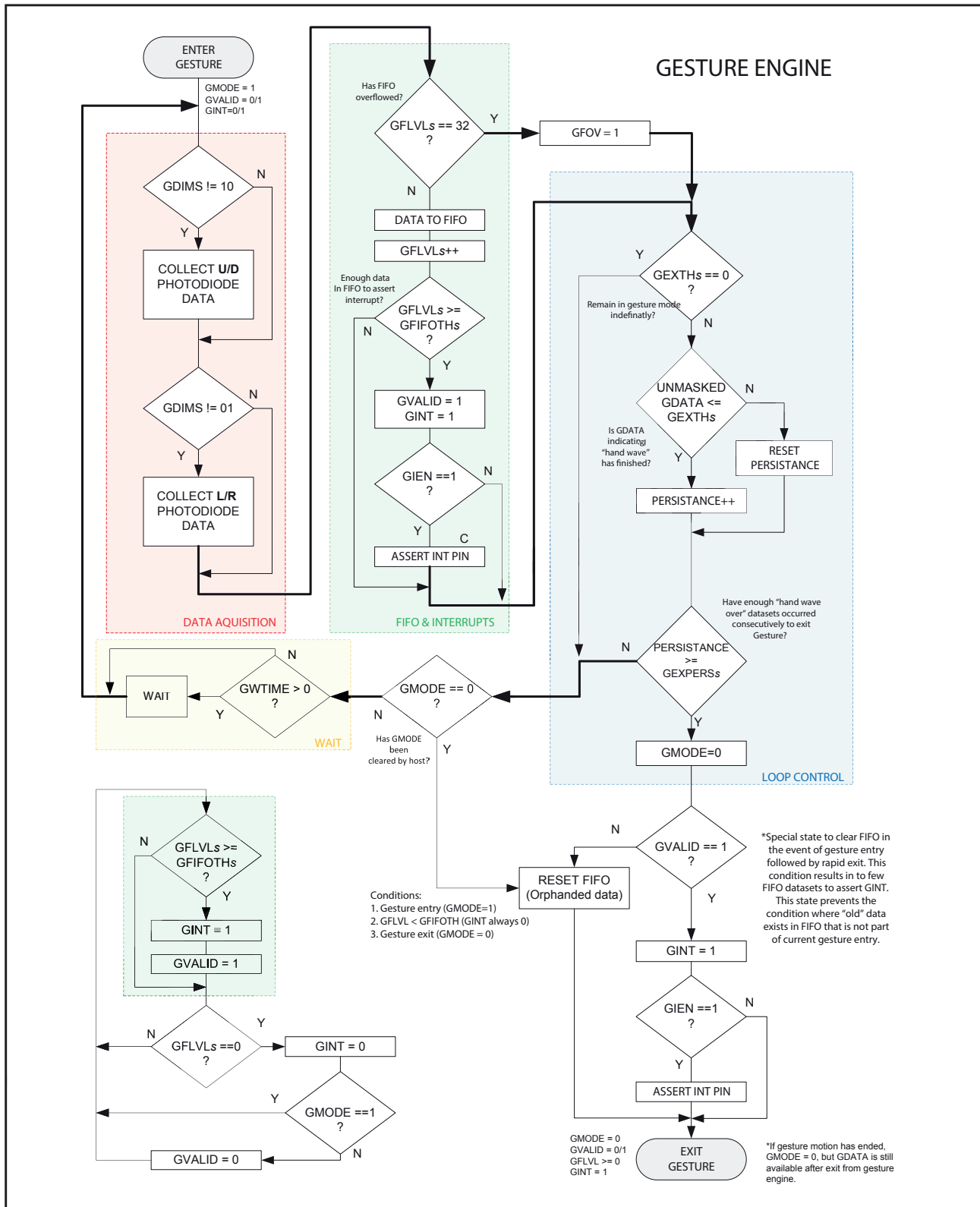


Figure 10. Detailed Gesture Diagram

Gesture results are affected by three fundamental factors: IR LED emission, IR reception, and environmental factors, including motion.

During operation, the Gesture engine is entered when its enable bit, GEN, and the operating mode bit, GMODE, are both set. GMODE can be set/reset manually, via I²C, or becomes set when proximity results, PDATA, is greater or equal to the gesture proximity entry threshold, GPENTH. Exit of the gesture engine will not occur until GMODE is reset to zero. During normal operation, GMODE is reset when all 4-bytes of a gesture dataset fall below the exit threshold, GEXTH, for GEXPERS times. This exit condition is also influenced by the gesture exit mask, GEXMSK, which includes all non-masked datum (i.e. singular 1-byte U, D, L, R points). To prevent premature exit, a persistence filter is also included; exit will only occur if a consecutive number of below-threshold results is greater or equal to the persistence value, GEXPERS. Each dataset result that is above-threshold will reset the persistence count. False or incomplete gestures (engine entry and exit without GVALID transitioning high) will not generate a gesture interrupt, GINT, and FIFO data will automatically be purged.

Once in operating inside the gesture engine, the IR reception signal path begins with IR detection at the photodiodes and ends with the four, 8-bit gesture results corresponding to accumulated signal strength on each diode. Signal from the four photodiodes is amplified, and offset adjusted to optimize performance. Photodiodes are paired to form two signal paths: UP/DOWN and LEFT/RIGHT. Photodiode pairs can be masked to exclude its results from the gesture FIFO data. For example, if only UP-DOWN motions detection is required the gesture dimension control bits, GDIMS, may be set to 0x01. FIFO data will be zero for RIGHT/LEFT results and accumulation/ADC integration time will be approximately halved. Gain is adjustable from

1x to 8x using the GGAIN control bits. Offset correction is accomplished by individual adjustment to GOFFSET_U, GOFFSET_D, GOFFSET_L, GOFFSET_R registers to improve cross-talk performance. The analog circuitry of the device applies offset values as a subtraction to the signal accumulation; therefore a positive offset value has the effect of decreasing the results.

Optically, the IR emission appears as a pulse train. The number of pulses is set by the GPULSE bits and the period of each pulse is adjustable using the GPLEN bits. Pulse train repetition (i.e. the circular flow of operation inside the gesture state machine) can be delayed by setting a non-zero value in the gesture wait time bits, GWTIME. The inclusion of a wait state reduces the both the power consumption and the data rate.

The intensity of the IR emission is selectable using the GLDRIVE control bits; corresponding to four, factory calibrated, current levels. If a higher intensity is required (E.g. longer detection distance or device placement beneath dark glass) then the LEDBOOST bit can be used to boost current up to an additional 300%.

The current consumption of the integrated IR LED is shown in Table 5. (Three examples at various LED drive settings)

Table 5. Simplified Power Calculation

| | Case 1 | Case 2 | Case 3 |
|----------------------------------|--------|--------|--------|
| ILED (mA) | 100 | 150 | 300 |
| GPULSE (no of pulses) | 8 | 8 | 8 |
| GPLEN (us) | 16 | 16 | 32 |
| GWTIME (No of wait state) | 2 | 2 | 1 |
| Total Current (mA) | 3.76 | 5.49 | 16.14 |

An interrupt is generated based on the number of gesture “datasets” results placed in the FIFO. A dataset is defined as 4-byte directional data corresponding to U-D-L-R. The FIFO can buffer up to 32 datasets before it overflows. If the FIFO overflows (host did not read quickly enough) then the most recent data will be lost. If the FIFO level, GFLVL, becomes greater or equal to the threshold value set by GFIFOTH, then the GVALID bit is set, indicating valid data is available; the gesture interrupt bit, GINT, is asserted, and if GIEN bit is set a hardware interrupt on the INT pin will also assert. Before exit of gesture engine, one final interrupt will always occur if GVALID is asserted, signaling data remains in the FIFO. Gesture Interrupts flags: GINT, GVALID, and GFLVL are cleared by emptying FIFO (i.e., all data has been read).

The correlation of motion to FIFO data and direction characteristics) is not obvious at first glance. As depicted in Figure 12, the four directional sensors are placed in an orthogonal pattern optically lensed aperture. Diodes are designated as: U, D, L, R; the 8-bit results corresponding to each diode is available at the following sequential FIFO locations: 0xFC, 0xFD, 0xFE, and 0xFF.

Ideally, gesture detection works by capturing and comparing the amplitude and phase difference between directional sensor results. The directional sensors are arranged such that the diode opposite to the directional motion receives a larger portion of the reflected IR signal upon entry, then a smaller portion upon exit. In the example illustration, a downward or rightward motion of a target is illustrated per the respective arrows in Figure 11.

Directional Orientation

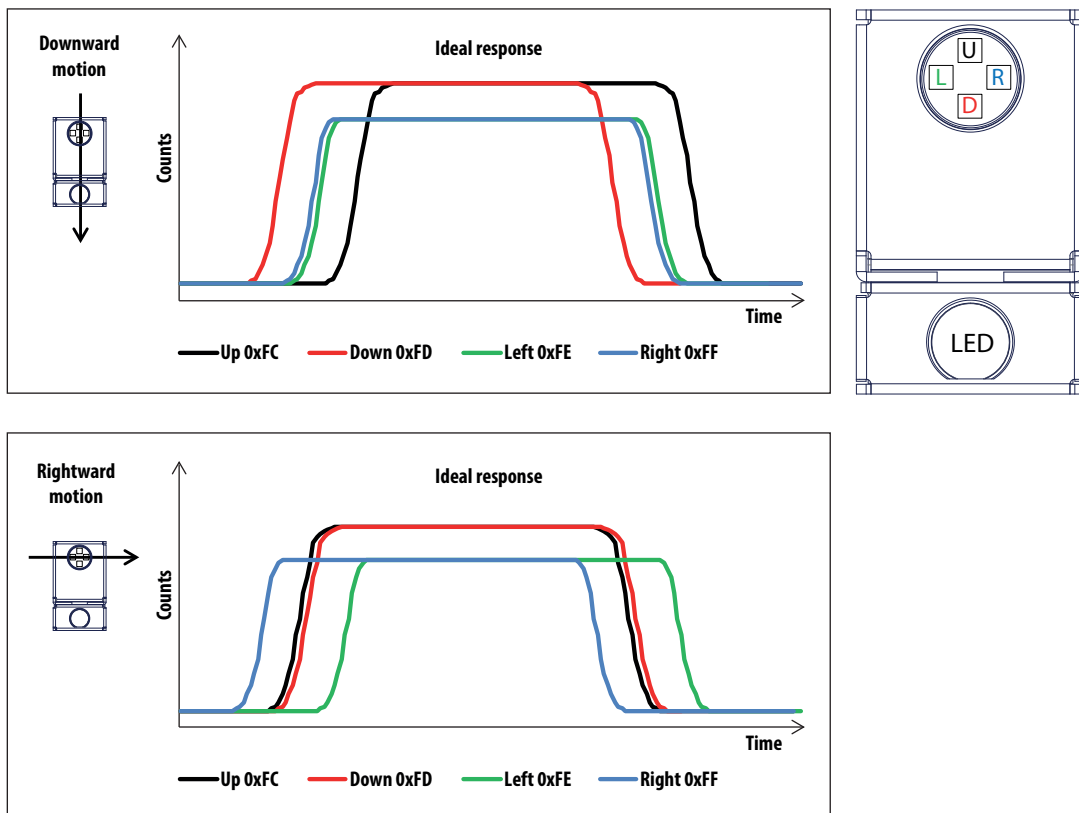


Figure 11. Directional Orientation

Optical and Mechanical Design Consideration

Optical Transmittance of Window Material

Windows with an IR transmittance of at least 80% (measured at 950 nm) are recommended for use with the APDS-9960. Note that for aesthetic reasons, the window's material could be tinted or coated with a dark ink. For example, a 20% (measured at 550 nm) visible transmittance window with 80% IR transmittance can be used. Such a coating would have transmittance spectral response with low transmittance within the visible range and a high transmittance in the infrared range. This low to high transmittance transition wavelength should be shorter than 650 nm to minimize crosstalk.

Examples of recommended window material part numbers are shown in Table 6.

Table 6. Recommended Plastic Materials

| Material number | Visible light transmission | Refractive index |
|-----------------|----------------------------|------------------|
| Makrolon LQ2647 | 87% | 1.587 |
| Makrolon LQ3147 | 87% | 1.587 |
| Makrolon LQ3187 | 85% | 1.587 |
| Lexan OQ92S | 88 - 90% | - |
| Lexan OQ4120R | 88 - 90% | 1.586 |
| Lexan OQ4320R | 88 - 90% | 1.586 |

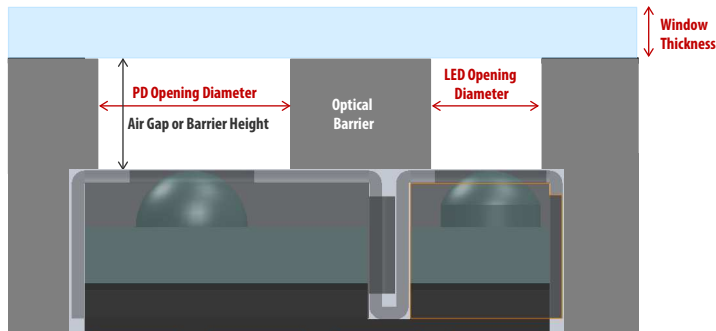


Figure 12. Rubber Barrier

Crosstalk and Window Air Gap

Crosstalk is PS or Gesture output caused by unwanted LED IR rays reflection without any object present. To control crosstalk when operating the sensor in gesture mode, we recommend that a rubber isolating barrier be fitted over the sensor. A possible design is shown in Figure 12.

The rubber consists of two cylindrical openings, one for the LED and the other for the Photodetector. The window thickness should not be more than 1 mm. When assembled the rubber barrier should form a good optical seal to the bottom of the window.

Recommended dimensions of the barrier are:

| Air Gap | PD Opening Diameter | LED Opening Diameter |
|---------|---------------------|----------------------|
| 1 mm | 2 mm | 1.5 mm |

Residual crosstalk of the Up, Down, Left and Right Gesture output may be reduced by writing to the individual GOFFSET registers. Such calibration is necessary to ensure good gesture sensing performance.

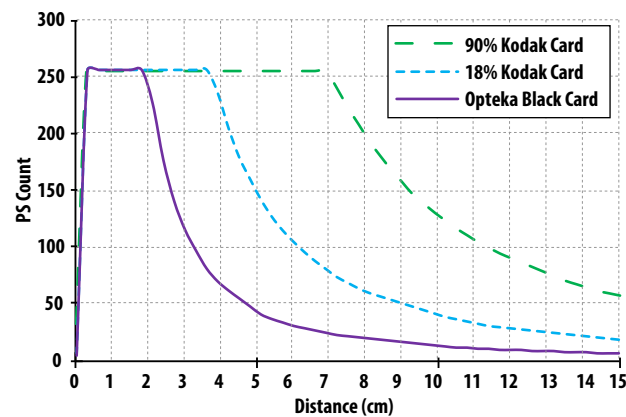


Figure 13a. PS Output vs. Distance at LDRIVE = 100 mA, PPULSE = 8, PGAIN = 4x, PPLEN = 8 μ s, LED_BOOST = 100% with various objects. No glass in front of the module

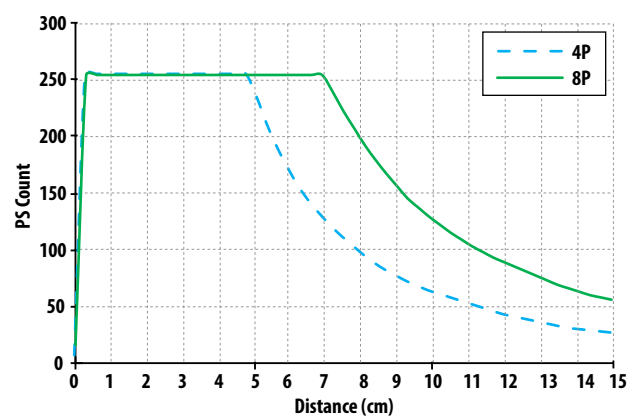


Figure 13b. PS Output vs. Distance at LDRIVE = 100 mA, PGAIN = 4x, PPLEN = 8 μ s, LED_BOOST = 100% with various pulses. No glass in front of the module

Register Set

The APDS-9960 is controlled and monitored by data registers and a command register accessed through the serial interface. These registers provide for a variety of control functions and can be read to determine results of the ADC conversions.

| Address | Register Name | Type | Register Function | Reset Value |
|-------------|---------------|------|--|-------------|
| 0x00 – 0x7F | RAM | R/W | RAM | 0x00 |
| 0x80 | ENABLE | R/W | Enable states and interrupts | 0x00 |
| 0x81 | ATIME | R/W | ADC integration time | 0xFF |
| 0x83 | WTIME | R/W | Wait time (non-gesture) | 0xFF |
| 0x84 | AILTL | R/W | ALS interrupt low threshold low byte | -- |
| 0x85 | AILTH | R/W | ALS interrupt low threshold high byte | -- |
| 0x86 | AIHTL | R/W | ALS interrupt high threshold low byte | 0x00 |
| 0x87 | AIHTH | R/W | ALS interrupt high threshold high byte | 0x00 |
| 0x89 | PILT | R/W | Proximity interrupt low threshold | 0x00 |
| 0x8B | PIHT | R/W | Proximity interrupt high threshold | 0x00 |
| 0x8C | PERS | R/W | Interrupt persistence filters (non-gesture) | 0x00 |
| 0x8D | CONFIG1 | R/W | Configuration register one | 0x60 |
| 0x8E | PPULSE | R/W | Proximity pulse count and length | 0x40 |
| 0x8F | CONTROL | R/W | Gain control | 0x00 |
| 0x90 | CONFIG2 | R/W | Configuration register two | 0x01 |
| 0x92 | ID | R | Device ID | ID |
| 0x93 | STATUS | R | Device status | 0x00 |
| 0x94 | CDATAAL | R | Low byte of clear channel data | 0x00 |
| 0x95 | CDATAH | R | High byte of clear channel data | 0x00 |
| 0x96 | RDATAAL | R | Low byte of red channel data | 0x00 |
| 0x97 | RDATAH | R | High byte of red channel data | 0x00 |
| 0x98 | GDATAAL | R | Low byte of green channel data | 0x00 |
| 0x99 | GDATAH | R | High byte of green channel data | 0x00 |
| 0x9A | BDATAAL | R | Low byte of blue channel data | 0x00 |
| 0x9B | BDATAH | R | High byte of blue channel data | 0x00 |
| 0x9C | PDATA | R | Proximity data | 0x00 |
| 0x9D | POFFSET_UR | R/W | Proximity offset for UP and RIGHT photodiodes | 0x00 |
| 0x9E | POFFSET_DL | R/W | Proximity offset for DOWN and LEFT photodiodes | 0x00 |
| 0x9F | CONFIG3 | R/W | Configuration register three | 0x00 |
| 0xA0 | GPENTH | R/W | Gesture proximity enter threshold | 0x00 |
| 0xA1 | GEXTH | R/W | Gesture exit threshold | 0x00 |
| 0xA2 | GCONF1 | R/W | Gesture configuration one | 0x00 |
| 0xA3 | GCONF2 | R/W | Gesture configuration two | 0x00 |
| 0xA4 | GOFFSET_U | R/W | Gesture UP offset register | 0x00 |
| 0xA5 | GOFFSET_D | R/W | Gesture DOWN offset register | 0x00 |
| 0xA7 | GOFFSET_L | R/W | Gesture LEFT offset register | 0x00 |
| 0xA9 | GOFFSET_R | R/W | Gesture RIGHT offset register | 0x00 |
| 0xA6 | GPULSE | R/W | Gesture pulse count and length | 0x40 |
| 0xAA | GCONF3 | R/W | Gesture configuration three | 0x00 |
| 0xAB | GCONF4 | R/W | Gesture configuration four | 0x00 |
| 0xAE | GFLVL | R | Gesture FIFO level | 0x00 |
| 0xAF | GSTATUS | R | Gesture status | 0x00 |
| 0xE4 (1) | IFORCE | W | Force interrupt | 0x00 |
| 0xE5 (1) | PICLEAR | W | Proximity interrupt clear | 0x00 |
| 0xE6 (1) | CICLEAR | W | ALS clear channel interrupt clear | 0x00 |
| 0xE7 (1) | AICLEAR | W | All non-gesture interrupts clear | 0x00 |
| 0xFC | GFIFO_U | R | Gesture FIFO UP value | 0x00 |
| 0xFD | GFIFO_D | R | Gesture FIFO DOWN value | 0x00 |
| 0xFE | GFIFO_L | R | Gesture FIFO LEFT value | 0x00 |
| 0xFF | GFIFO_R | R | Gesture FIFO RIGHT value | 0x00 |

Note

1. Interrupt clear and force registers require a special I2C “address accessing” transaction. Please refer to the Register Description section for details.

Enable Register (0x80)

The ENABLE register is used to power the device on/off, enable functions and interrupts.

| Field | Bits | Description |
|----------|------|---|
| Reserved | 7 | Reserved. Write as 0. |
| GEN | 6 | Gesture Enable. When asserted, the gesture state machine can be activated. Activation is subject to the states of PEN and GMODE bits. |
| PIEN | 5 | Proximity Interrupt Enable. When asserted, it permits proximity interrupts to be generated, subject to the persistence filter settings. |
| AIEN | 4 | ALS Interrupt Enable. When asserted, it permits ALS interrupts to be generated, subject to the persistence filter settings. |
| WEN | 3 | Wait Enable. This bit activates the wait feature. Writing a one activates the wait timer. Writing a zero disables the wait timer. |
| PEN | 2 | Proximity Detect Enable. This field activates the proximity detection. Writing a one activates the proximity. Writing a zero disables the proximity. |
| AEN | 1 | ALS Enable. This field activates ALS function. Writing a one activates the ALS. Writing a zero disables the ALS. |
| PON | 0 | Power ON. This field activates the internal oscillator to permit the timers and ADC channels to operate. Writing a one activates the oscillator. Writing a zero disables the oscillator and puts the device into a low power sleep mode. During reads and writes over the I2C interface, this bit is temporarily overridden and the oscillator is enabled, independent of the state of PON. |

Note: Before enabling Gesture, Proximity, or ALS, all of the bits associated with control of the desired function must be set. Changing control register values while operating may result in invalid results.

ADC Integration Time Register (0x81)

The ATIME register controls the internal integration time of ALS/Color analog to digital converters. Upon power up, the ADC integration time register is set to 0xFF.

The maximum count (or saturation) value can be calculated based upon the integration time and the size of the count register (i.e. 16 bits). For ALS/Color, the maximum count will be the lesser of either:

- 65535 (based on the 16 bit register size) or
- The result of equation: $\text{CountMAX} = 1025 \times \text{CYCLES}$

| Field | Bits | Description | | | |
|-------|------|------------------------|---------------|-------------|------------------|
| ATIME | 7:0 | FIELD VALUE | CYCLES | TIME | MAX COUNT |
| | | 0 | 256 | 712 ms | 65535 |
| | | 182 | 72 | 200 ms | 65535 |
| | | = 256 – TIME / 2.78 ms | ... | ... | ... |
| | | 219 | 37 | 103 ms | 37889 |
| | | 246 | 10 | 27.8 ms | 10241 |
| | | 255 | 1 | 2.78 ms | 1025 |

Note: The ATIME register is only applicable to ALS/Color engine (16-bit data). The integration time for the 8-bit Proximity/Gesture engine, is a factor of four less than the nominal time (2.78ms), resulting in a fixed time of 0.696ms.

Wait Time Register (0x83)

The WTIME controls the amount of time in a low power mode between Proximity and/or ALS cycles. It is set 2.78ms increments unless the WLONG bit is asserted in which case the wait times are 12× longer. WTIME is programmed as a 2's complement number. Upon power up, the wait time register is set to 0xFF.

| Field | Bits | Description | | | |
|-------|------|------------------------|------------------|-------------------------|-------------------------|
| WTIME | 7:0 | FIELD VALUE | WAIT TIME | TIME (WLONG = 0) | TIME (WLONG = 1) |
| | | 0 | 256 | 712 ms | 8.54 s |
| | | = 256 – TIME / 2.78 ms | ... | ... | |
| | | 171 | 85 | 236 ms | 2.84 s |
| | | 255 | 1 | 2.78 ms | 0.03 s |

Notes:

1. The wait time register should be configured before AEN and/or PEN is asserted.
2. During any Proximity and/or ALS cycle, the wait state, depicted in the functional block diagram, is entered. For example, Prox only, Prox and ALS, or ALS only cycles always enter the WAIT state and are separated by the time defined by WTIME.

ALS Interrupt Threshold Register (0x84 – 0x87)

ALS level detection uses data generated by the Clear Channel. The ALS Interrupt Threshold registers provide 16-bit values to be used as the high and low thresholds for comparison to the 16-bit CDATA values. If AIEN is enabled and CDATA is greater than AILTH/AIHTH or less than AILTL/AIHTL for the number of consecutive samples specified in APERS an interrupt is asserted on the interrupt pin.

| Field | Address | Bits | Description |
|-------|---------|------|---|
| AILTL | 0x84 | 7:0 | This register provides the low byte of the low interrupt threshold. |
| AILTH | 0x85 | 7:0 | This register provides the high byte of the low interrupt threshold. |
| AIHTL | 0x86 | 7:0 | This register provides the low byte of the high interrupt threshold. |
| AIHTH | 0x87 | 7:0 | This register provides the high byte of the high interrupt threshold. |

Proximity Interrupt Threshold Register (0x89/0x8B)

The Proximity Interrupt Threshold Registers set the high and low trigger points for the comparison function which generates an interrupt. If PDATA, the value generated by proximity channel, crosses below the lower threshold specified, or above the higher threshold, an interrupt may be signaled to the host processor. Interrupt generation is subject to the value set in persistence (PERS).

| Field | Address | Bits | Description |
|-------|---------|------|--|
| PILT | 0x89 | 7:0 | This register provides the low interrupt threshold. |
| PIHT | 0x8B | 7:0 | This register provides the high interrupt threshold. |

Persistence Register (0x8C)

The Interrupt Persistence Register sets a value which is compared with the accumulated amount of ALS or Proximity cycles in which results were outside threshold values. Any Proximity or ALS result that is inside threshold values resets the count.

Separate counters are provided for proximity and ALS persistence detection.

| Field | Bits | Description | | | |
|-------|--|--|--|--|--|
| PPERS | 7:4 | Proximity Interrupt Persistence. Controls rate of proximity interrupt to the host processor. | | | |
| | | FIELD VALUE | INTERRUPT GENERATED WHEN... | | |
| | | 0 | Every proximity cycle | | |
| | | 1 | Any proximity value outside of threshold range | | |
| | | 2 | 2 consecutive proximity values out of range | | |
| | | 3 | 3 consecutive proximity values out of range | | |
| | | ... | ... | | |
| | | 15 | 15 consecutive proximity values out of range | | |
| | | APERS | 3:0 | ALS Interrupt Persistence. Controls rate of Clear channel interrupt to the host processor. | |
| | | | | FIELD VALUE | INTERRUPT GENERATED WHEN... |
| | | | | 0 | Every ALS cycle |
| | | | | 1 | Any ALS value outside of threshold range |
| | | | | 2 | 2 consecutive ALS values out of range |
| | | | | 3 | 3 consecutive ALS values out of range |
| | | | | 4 | 5 ... |
| | | | | 5 | 10 ... |
| 6 | 15 ... | | | | |
| 7 | 20 ... | | | | |
| 8 | 25 ... | | | | |
| 9 | 30 ... | | | | |
| 10 | 35 ... | | | | |
| 11 | 40 ... | | | | |
| 12 | 45 ... | | | | |
| 13 | 50 ... | | | | |
| 14 | 55 ... | | | | |
| 15 | 60 consecutive ALS values out of range | | | | |

Configuration Register One (0x8D)

The CONFIG1 register sets the wait long time. The register is set to 0x40 at power up.

| Field | Bits | Description |
|----------|------|---|
| Reserved | 7 | Reserved. Write as 0. |
| Reserved | 6 | Reserved. Write as 1. |
| Reserved | 5 | Reserved. Write as 1. |
| Reserved | 4 | Reserved. Write as 0. |
| Reserved | 3 | Reserved. Write as 0. |
| Reserved | 2 | Reserved. Write as 0. |
| WLONG | 1 | Wait Long. When asserted, the wait cycle is increased by a factor 12x from that programmed in the WTIME register. |
| Reserved | 0 | Reserved. Write as 0. |

Notes:

1. Bit 6 is reserved, and is automatically set to 1 at POR.
2. Bit 5 is reserved, and is automatically set to 1 at POR. If this bit is not set, power consumption will increase during wait states.

Proximity Pulse Count Register (0x8E)

The Proximity Pulse Count Register sets Pulse Width Modified current during a Proximity Pulse. The proximity pulse count register bits set the number of pulses to be output on the LDR pin. The Proximity Length register bits set the amount of time the LDR pin is sinking current during a proximity pulse.

| Field | Bits | Description |
|--------------------------|------|---|
| PPLEN | 7:6 | Proximity Pulse Length. Sets the LED-ON pulse width during a proximity LDR pulse. |
| | | FIELD VALUE PULSE LENGTH |
| | | 0 4 μ s |
| | | 1 8 μ s (default) |
| | | 2 16 μ s |
| PPULSE | 5:0 | Proximity Pulse Count. Specifies the number of proximity pulses to be generated on LDR. Number of pulses is set by PPULSE value plus 1. |
| | | FIELD VALUE NUMBER OF PULSES |
| | | 0 1 |
| | | 1 2 |
| | | 2 3 |
| | | |
| 63 64 | | |

Notes:

1. The time described by PPLEN is the actual signal integration time. The LED will be activated slightly longer (typically 1.36 μ s) than the integration time.
2. The Proximity Pulse Count Register resets to 0x40

Control Register One (0x8F)

| Field | Bits | Description | | | | | | | | | | |
|-------------|-------------|---|-------------|-------------|---|--------|---|-------|---|-------|---|---------|
| LDRIVE | 7:6 | LED Drive Strength. <table border="1"><thead><tr><th>FIELD VALUE</th><th>LED CURRENT</th></tr></thead><tbody><tr><td>0</td><td>100 mA</td></tr><tr><td>1</td><td>50 mA</td></tr><tr><td>2</td><td>25 mA</td></tr><tr><td>3</td><td>12.5 mA</td></tr></tbody></table> | FIELD VALUE | LED CURRENT | 0 | 100 mA | 1 | 50 mA | 2 | 25 mA | 3 | 12.5 mA |
| FIELD VALUE | LED CURRENT | | | | | | | | | | | |
| 0 | 100 mA | | | | | | | | | | | |
| 1 | 50 mA | | | | | | | | | | | |
| 2 | 25 mA | | | | | | | | | | | |
| 3 | 12.5 mA | | | | | | | | | | | |
| Reserved | 5 | Reserved. Write as 0. | | | | | | | | | | |
| Reserved | 4 | Reserved. Write as 0. | | | | | | | | | | |
| PGAIN | 3:2 | Proximity Gain Control. <table border="1"><thead><tr><th>FIELD VALUE</th><th>GAIN VALUE</th></tr></thead><tbody><tr><td>0</td><td>1x</td></tr><tr><td>1</td><td>2x</td></tr><tr><td>2</td><td>4x</td></tr><tr><td>3</td><td>8x</td></tr></tbody></table> | FIELD VALUE | GAIN VALUE | 0 | 1x | 1 | 2x | 2 | 4x | 3 | 8x |
| FIELD VALUE | GAIN VALUE | | | | | | | | | | | |
| 0 | 1x | | | | | | | | | | | |
| 1 | 2x | | | | | | | | | | | |
| 2 | 4x | | | | | | | | | | | |
| 3 | 8x | | | | | | | | | | | |
| AGAIN | 1:0 | ALS and Color Gain Control. <table border="1"><thead><tr><th>FIELD VALUE</th><th>GAIN VALUE</th></tr></thead><tbody><tr><td>0</td><td>1x</td></tr><tr><td>1</td><td>4x</td></tr><tr><td>2</td><td>16x</td></tr><tr><td>3</td><td>64x</td></tr></tbody></table> | FIELD VALUE | GAIN VALUE | 0 | 1x | 1 | 4x | 2 | 16x | 3 | 64x |
| FIELD VALUE | GAIN VALUE | | | | | | | | | | | |
| 0 | 1x | | | | | | | | | | | |
| 1 | 4x | | | | | | | | | | | |
| 2 | 16x | | | | | | | | | | | |
| 3 | 64x | | | | | | | | | | | |

Configuration Register Two (0x90)

The Configuration Register Two independently enables or disables the saturation interrupts for Proximity and Clear channel. Saturation Interrupts are cleared by accessing the Clear Interrupt registers at 0xE5, 0xE6 and 0xE7. The LED_BOOST bits allow the LDR pin to sink more current above the maximum setting by LDRIVE and GLDRIVE.

| Field | Bits | Description | | | | | | | | | | |
|-------------|-------------------|---|-------------|-------------------|---|------|---|------|---|------|---|------|
| PSIEN | 7 | Proximity Saturation Interrupt Enable. 0 = Proximity saturation interrupt disabled 1 = Proximity saturation interrupt enabled | | | | | | | | | | |
| CPSIEN | 6 | Clear Photodiode Saturation Interrupt Enable. 0 = ALS Saturation Interrupt disabled 1 = ALS Saturation Interrupt enabled | | | | | | | | | | |
| LED_BOOST | 5:4 | Additional LDR current during proximity and gesture LED pulses. Current value, set by LDRIVE, is increased by the percentage of LED_BOOST. <table border="1"><thead><tr><th>FIELD VALUE</th><th>LED BOOST CURRENT</th></tr></thead><tbody><tr><td>0</td><td>100%</td></tr><tr><td>1</td><td>150%</td></tr><tr><td>2</td><td>200%</td></tr><tr><td>3</td><td>300%</td></tr></tbody></table> | FIELD VALUE | LED BOOST CURRENT | 0 | 100% | 1 | 150% | 2 | 200% | 3 | 300% |
| FIELD VALUE | LED BOOST CURRENT | | | | | | | | | | | |
| 0 | 100% | | | | | | | | | | | |
| 1 | 150% | | | | | | | | | | | |
| 2 | 200% | | | | | | | | | | | |
| 3 | 300% | | | | | | | | | | | |
| RESERVED | 3:1 | Reserved. Write as 0. | | | | | | | | | | |
| RESERVED | 0 | Reserved. Write as 1. Set high by default during POR. | | | | | | | | | | |

Note: A LED_BOOST value of 0 results in 100% of the current as set by LDRIVE (no additional current).

ID Register (0x92)

The read-only ID Register provides the device identification.

| Field | Bits | Description |
|-------|------|---|
| ID | 7:0 | Part number identification. 0xAB = APDS-9960 |

Status Register (0x93)

The read-only Status Register provides the status of the device. The register is set to 0x04 at power-up.

| Field | Bits | Description |
|----------|------|--|
| CPSAT | 7 | Clear Photodiode Saturation. When asserted, the analog sensor was at the upper end of its dynamic range. The bit can be de-asserted by sending a Clear channel interrupt command (0xE6 CICLEAR) or by disabling the ADC (AEN=0). This bit triggers an interrupt if CPSIEN is set. |
| PGSAT | 6 | Indicates that an analog saturation event occurred during a previous proximity or gesture cycle. Once set, this bit remains set until cleared by clear proximity interrupt special function command (0xE5 PICLEAR) or by disabling Prox (PEN=0). This bit triggers an interrupt if PSIEN is set. |
| PINT | 5 | Proximity Interrupt. This bit triggers an interrupt if PIEN in ENABLE is set. |
| AINT | 4 | ALS Interrupt. This bit triggers an interrupt if AIEN in ENABLE is set. |
| RESERVED | 3 | Do not care. |
| GINT | 2 | Gesture Interrupt. GINT is asserted when GFVLV becomes greater than GFIFOTH or if GVALID has become asserted when GMODE transitioned to zero. The bit is reset when FIFO is completely emptied (read). |
| PVALID | 1 | Proximity Valid. Indicates that a proximity cycle has completed since PEN was asserted or since PDATA was last read. A read of PDATA automatically clears PVALID. |
| AVALID | 0 | ALS Valid. Indicates that an ALS cycle has completed since AEN was asserted or since a read from any of the ALS/Color data registers. |

RGBC Data Register (0x94 – 0x9B)

Red, green, blue, and clear data is stored as 16-bit values. The read sequence must read byte pairs (low followed by high) starting on an even address boundary (0x94, 0x96, 0x98, or 0x9A) inside the RGBC Data Register block. When the lower byte register is read, the upper eight bits are stored into a shadow register, which is read by a subsequent read to the upper byte. The upper register will read the correct value even if additional ADC integration cycles end between the reading of the lower and upper registers.

| Field | Address | Bits | Description |
|--------|---------|------|----------------------------------|
| CDATAL | 0x94 | 7:0 | Low Byte of clear channel data. |
| CDATAH | 0x95 | 7:0 | High Byte of clear channel data. |
| RDATAL | 0x96 | 7:0 | Low Byte of red channel data. |
| RDATAH | 0x97 | 7:0 | High Byte of red channel data. |
| GDATAL | 0x98 | 7:0 | Low Byte of green channel data. |
| GDATAH | 0x99 | 7:0 | High Byte of green channel data. |
| BDATAL | 0x9A | 7:0 | Low Byte of blue channel data. |
| BDATAH | 0x9B | 7:0 | High Byte of blue channel data. |

Note: When reading register contents, a read of the lower byte data automatically latches the corresponding higher byte data (16 bit latch). This feature guarantees that the high byte value has not been updated by the ADC between I2C reads. In addition, reading CDATAL register not only latches CDATAH but also latches all eight RGBC register simultaneously (64 bit latch).

Proximity Data Register (0x9C)

Proximity data is stored as an 8-bit value.

| Field | Address | Bits | Description |
|-------|---------|------|-----------------|
| PDATA | 0x9C | 7:0 | Proximity data. |

Proximity Offset UP / RIGHT Register (0x9D)

In proximity mode, the UP and RIGHT photodiodes are connected forming a diode pair. The POFFSET_UR is an 8-bit value used to scale an internal offset correction factor to compensate for crosstalk in the application. This value is encoded in sign/magnitude format.

| Field | Bits | Description | |
|------------|------|--------------------|---------------------------------|
| POFFSET_UR | 7:0 | FIELD VALUE | Offset Correction Factor |
| | | 01111111 | 127 |
| | | ... | ... |
| | | 00000001 | 1 |
| | | 00000000 | 0 |
| | | 10000001 | -1 |
| | | ... | ... |
| | | 11111111 | -127 |

Proximity Offset DOWN / LEFT Register (0x9E)

In Proximity mode, the DOWN and LEFT photodiodes are connected forming a diode pair. The POFFSET_DL is an 8-bit value used to scale an internal offset correction factor to compensate for crosstalk in the application. This value is encoded in sign/magnitude format.

| Field | Bits | Description | |
|------------|------|--------------------|---------------------------------|
| POFFSET_DL | 7:0 | FIELD VALUE | Offset Correction Factor |
| | | 01111111 | 127 |
| | | ... | ... |
| | | 00000001 | 1 |
| | | 00000000 | 0 |
| | | 10000001 | -1 |
| | | ... | ... |
| | | 11111111 | -127 |

Configuration Three Register (0x9F)

The CONFIG3 register is used to select which photodiodes are used for proximity. Two photodiodes are paired to provide signal. In proximity mode, UP and RIGHT photodiodes are connected forming a diode pair; similarly the DOWN and LEFT photodiodes form a diode pair.

| Field | Bits | Description | | | | | | | | | | | | | | | | |
|----------------------|------|--|----------------------|------|------------|---|------------|---|------------|---|------------|---|------------|---|------------|---|------------|---|
| RESERVED | 7:6 | Reserved. Write as 0. | | | | | | | | | | | | | | | | |
| PCMP | 5 | Proximity Gain Compensation Enable. This bit provides gain compensation when proximity photodiode signal is reduced as a result of sensor masking. If only one diode of the diode pair is contributing, then only half of the signal is available at the ADC; this results in a maximum ADC value of 127. Enabling PCMP enables an additional gain of 2X, resulting in a maximum ADC value of 255. | | | | | | | | | | | | | | | | |
| | | <table border="1"> <thead> <tr> <th>PMASK_X (U, D, L, R)</th> <th>PCMP</th> </tr> </thead> <tbody> <tr> <td>0, 1, 1, 1</td> <td>1</td> </tr> <tr> <td>1, 0, 1, 1</td> <td>1</td> </tr> <tr> <td>1, 1, 0, 1</td> <td>1</td> </tr> <tr> <td>1, 1, 1, 0</td> <td>1</td> </tr> <tr> <td>0, 1, 0, 1</td> <td>1</td> </tr> <tr> <td>1, 0, 1, 0</td> <td>1</td> </tr> <tr> <td>All Others</td> <td>0</td> </tr> </tbody> </table> | PMASK_X (U, D, L, R) | PCMP | 0, 1, 1, 1 | 1 | 1, 0, 1, 1 | 1 | 1, 1, 0, 1 | 1 | 1, 1, 1, 0 | 1 | 0, 1, 0, 1 | 1 | 1, 0, 1, 0 | 1 | All Others | 0 |
| PMASK_X (U, D, L, R) | PCMP | | | | | | | | | | | | | | | | | |
| 0, 1, 1, 1 | 1 | | | | | | | | | | | | | | | | | |
| 1, 0, 1, 1 | 1 | | | | | | | | | | | | | | | | | |
| 1, 1, 0, 1 | 1 | | | | | | | | | | | | | | | | | |
| 1, 1, 1, 0 | 1 | | | | | | | | | | | | | | | | | |
| 0, 1, 0, 1 | 1 | | | | | | | | | | | | | | | | | |
| 1, 0, 1, 0 | 1 | | | | | | | | | | | | | | | | | |
| All Others | 0 | | | | | | | | | | | | | | | | | |
| SAI | 4 | Sleep After Interrupt. When enabled, the device will automatically enter low power mode when the INT pin is asserted and the state machine has progressed to the SAI decision block. Normal operation is resumed when INT pin is cleared over I2C. | | | | | | | | | | | | | | | | |
| PMASK_U | 3 | Proximity Mask UP Enable. Writing a 1 disables this photodiode. | | | | | | | | | | | | | | | | |
| PMASK_D | 2 | Proximity Mask DOWN Enable. Writing a 1 disables this photodiode. | | | | | | | | | | | | | | | | |
| PMASK_L | 1 | Proximity Mask LEFT Enable. Writing a 1 disables this photodiode. | | | | | | | | | | | | | | | | |
| PMASK_R | 0 | Proximity Mask RIGHT Enable. Writing a 1 disables this photodiode. | | | | | | | | | | | | | | | | |

Gesture Proximity Enter Threshold Register (0xA0)

The Gesture Proximity Enter Threshold Register value is compared with Proximity value, PDATA, to determine if the gesture state machine is entered. The proximity persistence filter, PPERS, is not used to determine gesture state machine entry.

| Field | Bits | Description |
|--------|------|--|
| GPENTH | 7:0 | Gesture Proximity Entry Threshold. This register sets the Proximity threshold value used to determine a "gesture start" and subsequent entry into the gesture state machine. |

Note: Bit 4 must be set to 0.

Gesture Exit Threshold Register (0xA1)

The Gesture Proximity Exit Threshold Register value compares all non-masked gesture detection photodiodes (UDLR). Gesture state machine exit is also governed by the value in the Gesture Exit Persistence register, GEPERS.

| Field | Bits | Description |
|-------|------|--|
| GEXTH | 7:0 | Gesture Exit Threshold. This register sets the threshold value used to determine a “gesture end” and subsequent exit of the gesture state machine. Setting GTHR_OUT to 0x00 will prevent gesture exit until GMODE is set to 0. |

Gesture Configuration One Register (0xA2)

The Gesture Configuration One Register contains settings that govern gesture detector masking, FIFO interrupt generation and gesture exit persistence filter.

| Field | Bits | Description |
|--|------|---|
| GFIFOTH | 7:6 | Gesture FIFO Threshold. This value is compared with the FIFO Level (i.e. the number of UDLR datasets) to generate an interrupt (if enabled). |
| | | FIELD VALUE THRESHOLD |
| | | 0 Interrupt is generated after 1 dataset is added to FIFO |
| | | 1 Interrupt is generated after 4 datasets are added to FIFO |
| | | 2 Interrupt is generated after 8 datasets are added to FIFO |
| GEXMSK | 5:2 | Gesture Exit Mask. Controls which of the gesture detector photodiodes (UDLR) will be included to determine a “gesture end” and subsequent exit of the gesture state machine. Unmasked UDLR data will be compared with the value in GTHR_OUT. Field value bits correspond to UDLR detectors. |
| | | FIELD VALUE EXIT MASK |
| | | 0000 All UDLR detector data will be included in sum |
| | | 0001 R detector data will not be included in sum |
| | | 0010 L detector data will not be included in sum |
| | | 0100 D detector data will not be included in sum |
| | | 1000 U detector data will not be included in sum |
| | | 0101 ... |
| | | 0110 L and D detector data will not be included in sum |
| | | 1111 All UDLR detector data will not be included in sum |
| GEXPERS | 1:0 | Gesture Exit Persistence. When a number of consecutive “gesture end” occurrences become equal or greater to the GEPERS value, the Gesture state machine is exited. |
| | | FIELD VALUE PERSISTENCE |
| | | 0 1st 'gesture end' occurrence results in gesture state machine exit. |
| | | 1 2nd 'gesture end' occurrence results in gesture state machine exit. |
| | | 2 4th 'gesture end' occurrence results in gesture state machine exit. |
| 3 7th 'gesture end' occurrence results in gesture state machine exit. | | |

Gesture Configuration Two Register (0xA3)

The Gesture Configuration Two register contains settings that govern wait time, LDR drive current strength and Gesture gain control. The GWTIME controls the amount of time in a low power mode between gesture detection cycles. GPDRIVE sets the LDR drive current strength governing LED intensity. GGAIN sets the analog gain associated with the photodiode output.

| Field | Bits | Description |
|--------------------------------|------|---|
| RESERVED | 7 | Reserved. Write as 0. |
| GGAIN | 6:5 | Gesture Gain Control. Sets the gain of the proximity receiver in gesture mode. |
| | | FIELD VALUE GAIN VALUE |
| | | 0 1x |
| | | 1 2x |
| | | 2 4x |
| 3 8x | | |
| GLDRIVE | 4:3 | Gesture LED Drive Strength. Sets LED Drive Strength in gesture mode. |
| | | FIELD VALUE LED CURRENT |
| | | 0 100 mA |
| | | 1 50 mA |
| | | 2 25 mA |
| 3 12.5 mA | | |
| GWTIME | 2:0 | Gesture Wait Time. The GWTIME controls the amount of time in a low power mode between gesture detection cycles. |
| | | FIELD VALUE WAIT TIME |
| | | 0 0 ms |
| | | 1 2.8 ms |
| | | 2 5.6 ms |
| | | 3 8.4 ms |
| | | 4 14.0 ms |
| | | 5 22.4 ms |
| | | 6 30.8 ms |
| 7 39.2 ms | | |

Notes:

1. The wait time register should be configured before GEN is asserted.
2. The time described by GTIME is the actual signal integration time. The LED will be activated slightly longer (typically 1.33 μ s) than the integration time.

Gesture UP Offset Register (0xA4)

The GOFFSET_U is an 8-bit value used to scale an internal offset correction factor to compensate for crosstalk in the application. This value is encoded in sign/magnitude format.

| Field | Bits | Description | |
|-----------|------|--------------------|---------------------------------|
| GOFFSET_U | 7:0 | FIELD VALUE | Offset Correction Factor |
| | | 01111111 | 127 |
| | | ... | ... |
| | | 00000001 | 1 |
| | | 00000000 | 0 |
| | | 10000001 | -1 |
| | | ... | ... |
| | | 11111111 | -127 |

Gesture DOWN Offset Register (0xA5)

The GOFFSET_D is an 8-bit value used to scale an internal offset correction factor to compensate for crosstalk in the application. This value is encoded in sign/magnitude format.

| Field | Bits | Description | |
|-----------|------|--------------------|---------------------------------|
| GOFFSET_D | 7:0 | FIELD VALUE | Offset Correction Factor |
| | | 01111111 | 127 |
| | | ... | ... |
| | | 00000001 | 1 |
| | | 00000000 | 0 |
| | | 10000001 | -1 |
| | | ... | ... |
| | | 11111111 | -127 |

Gesture LEFT Offset Register (0xA7)

The GOFFSET_L is an 8-bit value used to scale an internal offset correction factor to compensate for crosstalk in the application. This value is encoded in sign/magnitude format.

| Field | Bits | Description | |
|-----------|------|--------------------|---------------------------------|
| GOFFSET_L | 7:0 | FIELD VALUE | Offset Correction Factor |
| | | 01111111 | 127 |
| | | ... | ... |
| | | 00000001 | 1 |
| | | 00000000 | 0 |
| | | 10000001 | -1 |
| | | ... | ... |
| | | 11111111 | -127 |

Gesture RIGHT Offset Register (0xA9)

The GOFFSET_R is an 8-bit value used to scale an internal offset correction factor to compensate for crosstalk in the application. This value is encoded in sign/magnitude format.

| Field | Bits | Description | |
|-----------|------|---------------------------------|------|
| GOFFSET_L | 7:0 | FIELD VALUE | |
| | | Offset Correction Factor | |
| | | 01111111 | 127 |
| | | ... | ... |
| | | 00000001 | 1 |
| | | 00000000 | 0 |
| | | 10000001 | -1 |
| | | 11111111 | -127 |

Gesture Pulse Count and Length Register (0xA6)

The Gesture Pulse Count Register sets Pulse Width Modified current during a Gesture Pulse. The Gesture pulse count register bits set the number of pulses to be output on the LDR pin. The Gesture Length register bits set the amount of time the LDR pin is sinking current during a gesture pulse.

| Field | Bits | Description | |
|--------|------|--|-------------------------|
| GPLEN | 7:6 | Gesture Pulse Length. Sets the LED_ON pulse width during a Gesture LDR Pulse. | |
| | | FIELD VALUE | PULSE LENGTH |
| | | 0 | 4 μ s |
| | | 1 | 8 μ s (default) |
| | | 2 | 16 μ s |
| GPULSE | 5:0 | 3 | 32 μ s |
| | | Number of Gesture Pulses. Specifies the number of pulses to be generated on LDR. Number of pulses is set by GPULSE value plus 1. | |
| | | FIELD VALUE | Number OF PULSES |
| | | 0 | 1 |
| | | 1 | 2 |
| | | 2 | 3 |
| | | ... | ... |
| 63 | 64 | | |

Note:

1. The Gesture Pulse Count Register resets to 0x40 at initial power up (POR).

Gesture Configuration Three Register (0xAA)

The Gesture Configuration Three Register contains settings that govern which gesture photodiode pair: UP-DOWN and/or RIGHT-LEFT will be enabled (have valid data in FIFO) while the gesture state machine is collecting directional data. Normal mode enables all four gesture photodiodes and places data into FIFO as expected. Disabling a photodiode pair, essentially allows the enabled pair to collect data twice as fast. Data stored in the FIFO for a disabled pair is not valid. This feature is useful to improve reliability and accuracy of gesture detection when only one-dimensional gestures are expected.

| Field | Bits | Description |
|----------|--------------------|--|
| RESERVED | 7:2 | Reserved. Write as 0. |
| GDIMS | 1:0 | Gesture Dimension Select. Selects which gesture photodiode pairs are enabled to gather results during gesture. |
| | FIELD VALUE | GESTURE DIRECTION |
| | 0 | Both pairs are active. UP-DOWN and LEFT-RIGHT FIFO data is valid. |
| | 1 | Only the UP-DOWN pair is active. Ignore LEFT-RIGHT data in FIFO. |
| | 2 | Only the LEFT-RIGHT pair is active. Ignore UP-DOWN data in FIFO. |
| | 3 | Both pairs are active. UP-DOWN and LEFT-RIGHT FIFO data is valid. |

Gesture Configuration Four Register (0xAB)

The Gesture Configuration Four Register contains settings that govern Gesture interrupts and interrupt clearing/reset as well as operation mode control and status.

| Field | Bits | Description |
|-----------|------|--|
| RESERVED | 7:3 | Reserved. Write as 0. |
| GFIFO_CLR | 2 | Setting this bit to '1' clears GFIFO, GINT, GVALID, GFIFO_OV and GFIFO_LVL. |
| GIEN | 1 | Gesture interrupt enable. Gesture Interrupt Enable. When asserted, all gesture related interrupts are unmasked. |
| GMODE | 0 | Gesture Mode. Reading this bit reports if the gesture state machine is actively running, 1 = Gesture, 0= ALS, Proximity, Color. Writing a 1 to this bit causes immediate entry in to the gesture state machine (as if GPENTH had been exceeded). Writing a 0 to this bit causes exit of gesture when current analog conversion has finished (as if GEXTH had been exceeded). |

Gesture FIFO Level Register (0xAE)

The GFLVL Register indicates the number of datasets that are currently available in the FIFO for read. Reading a complete FIFO dataset (from address 0xFC to 0xFF) constitutes the reduction of the GPENTH register by one.

| Field | Bits | Description |
|-------|------|--|
| GFLVL | 7:0 | Gesture FIFO Level. This register indicates how many four byte data points - UDLR are ready for read over I2C. One four-byte dataset is equivalent to a single count in GFLVL. |

Gesture Status Register (0xAF)

The GSTATUS Register indicates the operational condition of the gesture state machine.

| Field | Bits | Description |
|----------|------|--|
| RESERVED | 7:2 | Do not care. |
| GFOV | 1 | Gesture FIFO Overflow. A setting of 1 indicates that the FIFO has filled to capacity and that new gesture detector data has been lost. |
| GVALID | 0 | Gesture FIFO Data. GVALID bit is sent when GFLVL becomes greater than GFIFOTH (i.e. FIFO has enough data to set GINT). GFIFOD is reset when GMODE = 0 and the GFLVL=0 (i.e., All FIFO data has been read). |

Note: If GINT (irrespective of GVALID) remains set after the FIFO has been read GFLVL times, this indicates that new data has been added to FIFO during the last FIFO read.

Clear Interrupt Registers (0xE4 – 0xE7)

Interrupts are cleared by “address accessing” the appropriate register. This is special I2C transaction consisting of only two bytes: chip address with R/W = 0, followed by a register address.

| Registers | Address | Bits | Description |
|-----------|---------|------|---|
| IFORCE | 0xE4 | 7:0 | Forces an interrupt (any value) |
| PICLEAR | 0xE5 | 7:0 | Proximity interrupt clear (any value) |
| CICLEAR | 0xE6 | 7:0 | ALS interrupt clear (any value) |
| AICLEAR | 0xE7 | 7:0 | Clears all non-gesture interrupts (any value) |

Gesture FIFO Register (0xFC – 0xFF)

In Gesture mode, the RAM area is repurposed as a 32 x 4 byte FIFO. Data is stored in four byte blocks. Each block, called a dataset, contains one integration cycle of UP, DOWN, LEFT, & RIGHT gesture data. Thirty-two separate datasets are stored within the FIFO before wrap-around overflow. If the FIFO overflows (i.e., 33 datasets before host/system can empty FIFO) new datasets will not replace existing datasets; instead an overflow flag will be set and new data will be lost.

Host/Systems acquire gesture data by reading addresses: 0xFC, 0xFD, 0xFE, & 0xFF, which directly correspond to UP, DOWN, LEFT, & RIGHT data points. Data can be read a single byte at a time (four consecutive I2C transactions) or by using a page read.

The internal FIFO read pointer and the FIFO Level register, GFLVL, values are updated when address 0xFF is accessed (single byte transactions) or when every fourth byte, corresponding to address 0xFF, is accessed in in page mode. If the FIFO continues to be accessed after GFLVL register is zero, dataset will be read as zero values.

The recommended procedure for reading data stored in the FIFO begins when a gesture interrupt is generated (GFLVL > GFIFOTH). Next, the host reads the FIFO Level register, GFLVL, to determine the amount of valid data in the FIFO.

Finally, the host begins to read address 0xFC (page read), and continues to read (clock-out data) until the FIFO is empty (Number of bytes is 4X GFLVL). For example, if GFLVL = 2, then the host should initiate a read at address 0xFC, and sequentially read all eight bytes. As the four-byte blocks are read, GFLVL register is decremented and the internal FIFO pointers are updated.

| Field | Address | Bits | Description |
|---------|---------|------|---------------------------|
| GFIFO_U | 0xFC | 7:0 | Gesture FIFO UP value. |
| GFIFO_D | 0xFD | 7:0 | Gesture FIFO DOWN value. |
| GFIFO_L | 0xFE | 7:0 | Gesture FIFO LEFT value. |
| GFIFO_R | 0xFF | 7:0 | Gesture FIFO RIGHT value. |

Application Information Hardware

In a proximity sensing system, the internal IR LED can be pulsed by more than 100 mA of rapidly switching current, therefore, a few design considerations must be kept in mind to get the best performance. The key goal is to reduce the power supply noise coupled back into the device during the LED pulses.

In many systems, there is a quiet analog supply and a noisy digital supply. By connecting the quiet supply to the VDD pin and the noisy supply to the LED, the key goal can be met. Place a $1\ \mu\text{F}$ low-ESR decoupling capacitor as close as possible to the VDD pin and another at the LEDA pin, along with a bulk storage capacitor ($\geq 10\ \mu\text{F}$) at the output of the LED voltage regulator to supply the current surge.

If operating from a single supply, use a $22\ \Omega$ resistor in series with the VDD supply line and a $1\ \mu\text{F}$ low ESR capacitor to filter any power supply noise. The previous capacitor placement considerations apply. However note that where LED current is boosted beyond 100 mA, it is recommended that the LEDA pin be connected to a separate power supply.

VBUS in the figures refers to the I²C-bus voltage. The I²C-bus signals and the Interrupt are open-drain outputs and require pull-up resistors. The pull-up resistor (R_p) value is a function of the I²C-bus speed, the I²C-bus voltage, and the capacitive load. A 10-k Ω pull-up resistor (R_{PI}) can be used for the interrupt line.

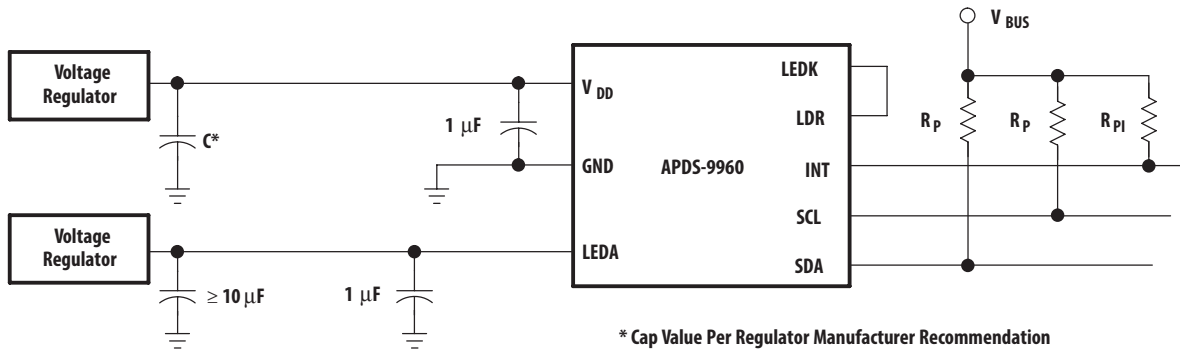


Figure 14a. Circuit Implementation using Separate Power Supplies

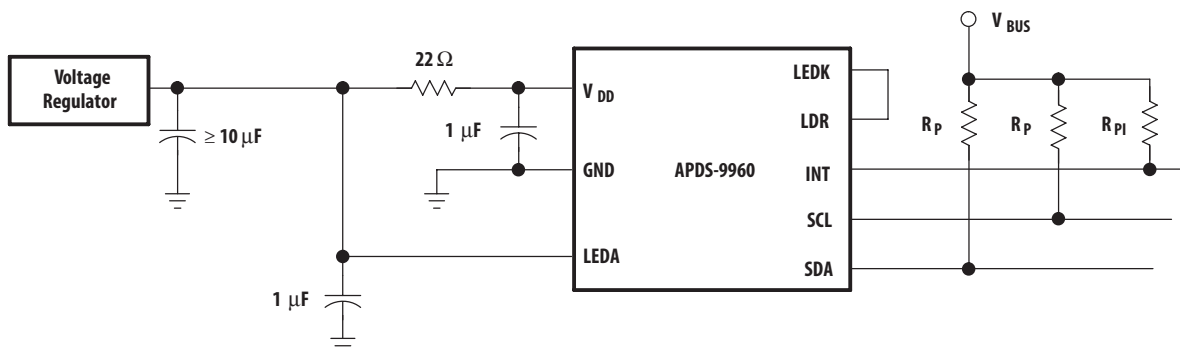
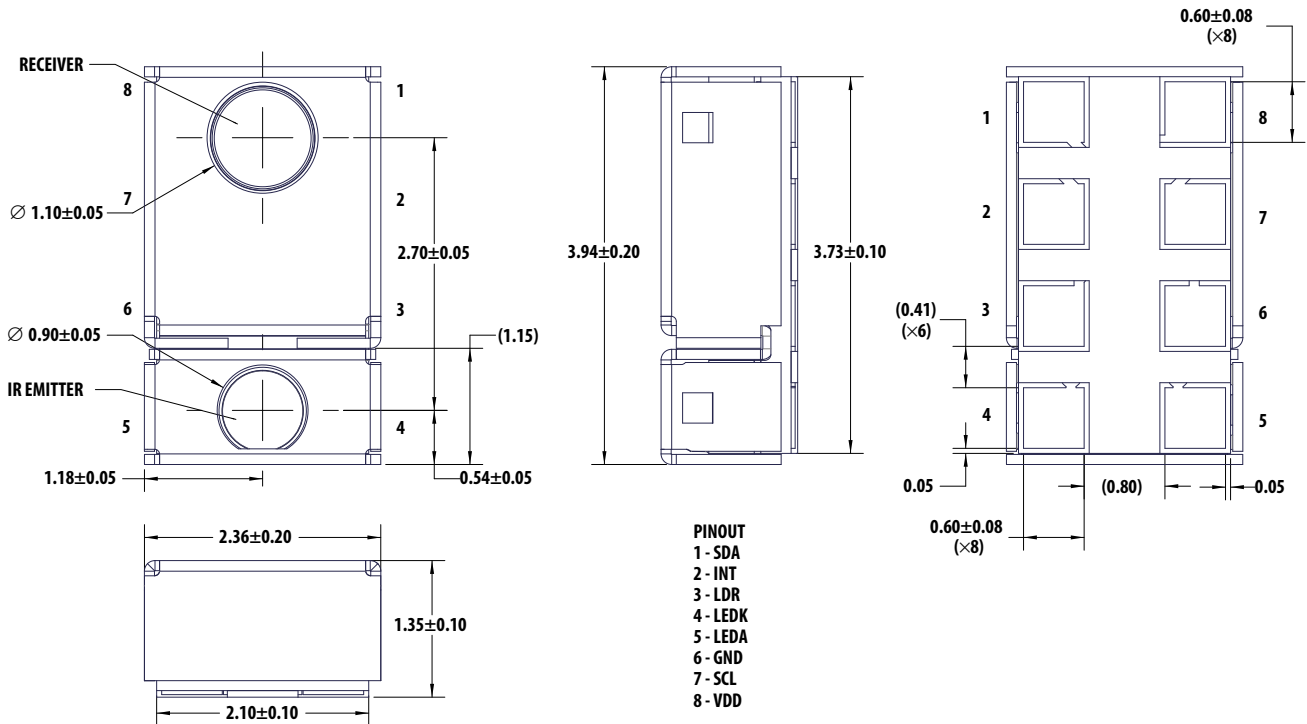


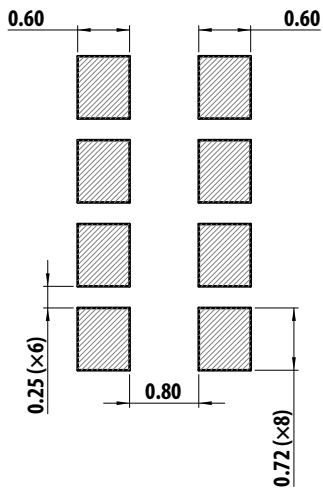
Figure 14b. Circuit Implementation using Single Power Supply

Package Outline Dimensions



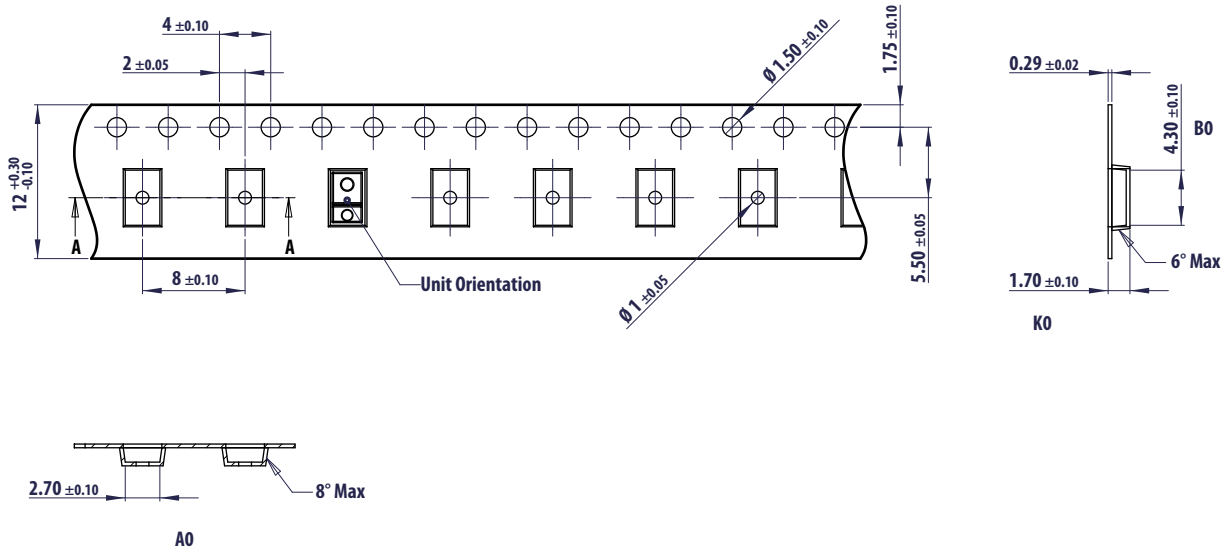
PCB Pad Layout

Suggested PCB pad layout guidelines for the Dual Flat No-Lead surface mount package are shown as follows:



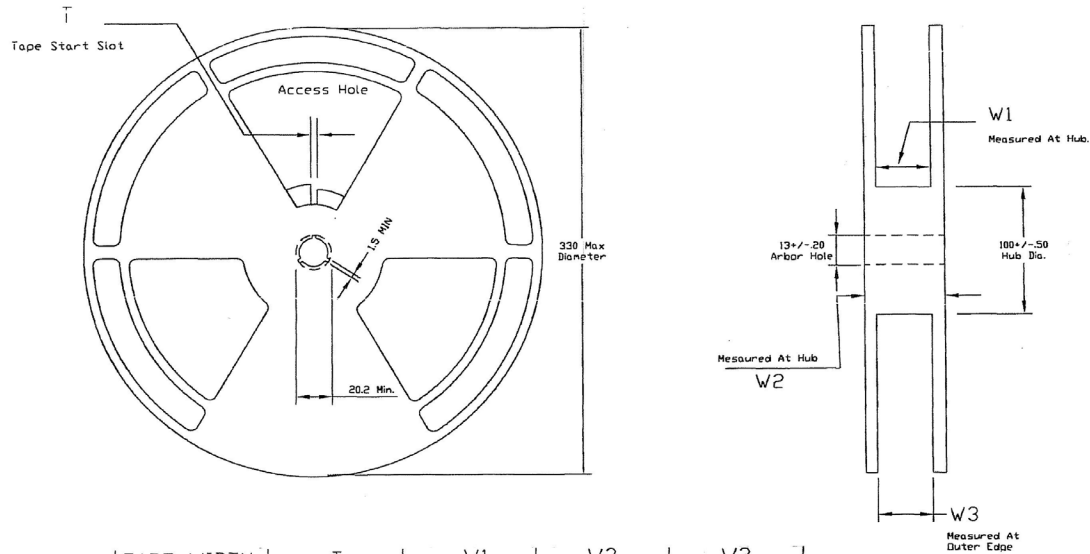
Note: All linear dimensions are in mm.

Tape Dimensions



Note: All linear dimensions are in mm.

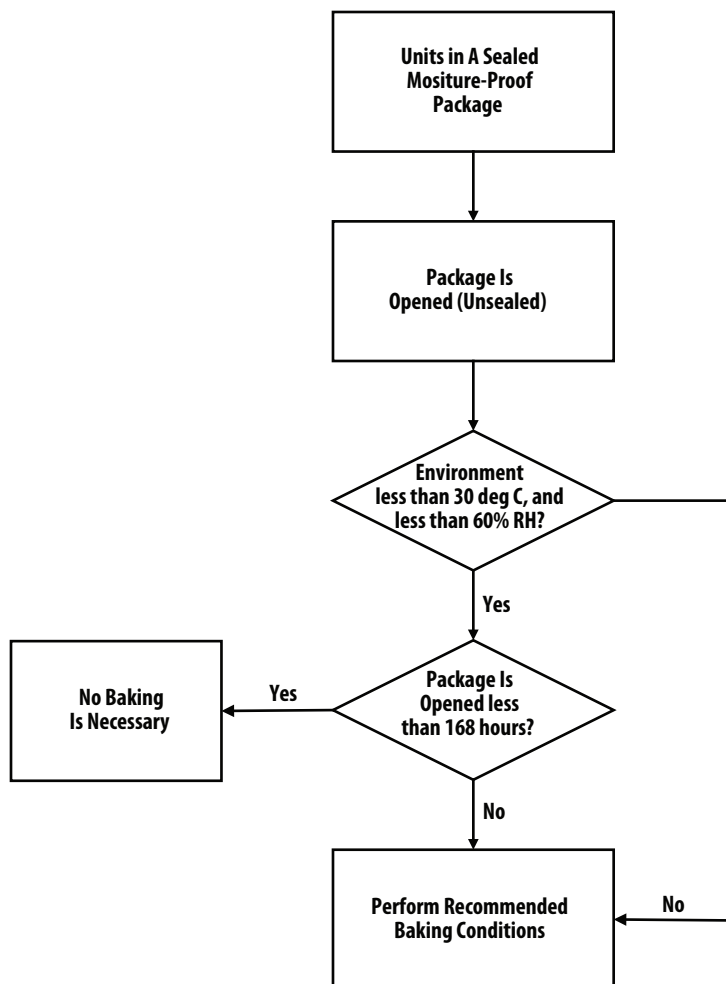
Reel Dimensions



| TAPE WIDTH | T | W1 | W2 | W3 |
|------------|--------------|----------------------|----------|--------------------|
| 12MM | 4 ± 0.50 | $12.4^{+2.0}_{-0.0}$ | 18.4 MAX | 11.9MIN 15.4MAX |

Moisture Proof Packaging

All APDS-9960 options are shipped in moisture proof package. Once opened, moisture absorption begins. This part is compliant to JEDEC MSL 3.



Baking Conditions

| Package | Temperature | Time |
|---------|-------------|----------|
| In Reel | 60 °C | 48 hours |
| In Bulk | 100 °C | 4 hours |

If the parts are not stored in dry conditions, they must be baked before reflow to prevent damage to the parts.

Baking should only be done once.

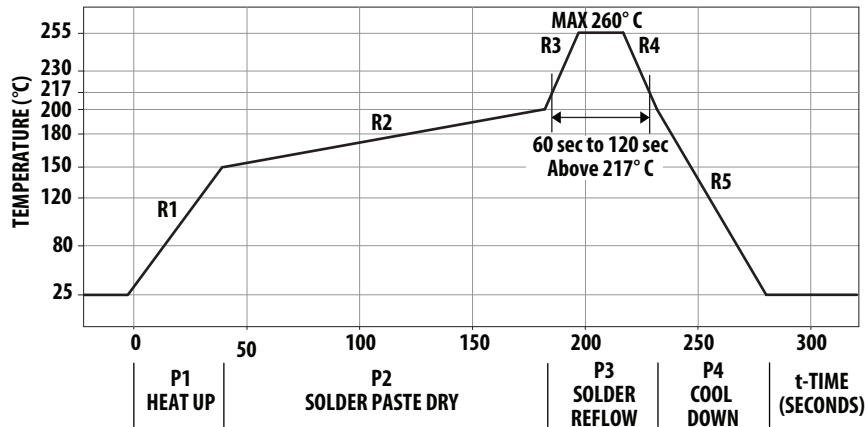
Recommended Storage Conditions

| | |
|---------------------|----------------|
| Storage Temperature | 10 °C to 30 °C |
| Relative Humidity | below 60% RH |

Time from unsealing to soldering

After removal from the bag, the parts should be soldered within 168 hours if stored at the recommended storage conditions. If times longer than 168 hours are needed, the parts must be stored in a dry box.

Recommended Reflow Profile



| Process Zone | Symbol | ΔT | Maximum $\Delta T/\Delta \text{time}$ or Duration |
|--|--------|------------------|---|
| Heat Up | P1, R1 | 25 °C to 150 °C | 3 °C/s |
| Solder Paste Dry | P2, R2 | 150 °C to 200 °C | 100 s to 180 s |
| Solder Reflow | P3, R3 | 200 °C to 260 °C | 3 °C/s |
| | P3, R4 | 260 °C to 200 °C | -6 °C/s |
| Cool Down | P4, R5 | 200 °C to 25 °C | -6 °C/s |
| Time maintained above liquidus point, 217 °C | | > 217 °C | 60 s to 120 s |
| Peak Temperature | | 260 °C | - |
| Time within 5 °C of actual Peak Temperature | | > 255 °C | 20 s to 40 s |
| Time 25 °C to Peak Temperature | | 25 °C to 260 °C | 8 mins |

The reflow profile is a straight-line representation of a nominal temperature profile for a convective reflow solder process. The temperature profile is divided into four process zones, each with different $\Delta T/\Delta \text{time}$ temperature change rates or duration. The $\Delta T/\Delta \text{time}$ rates or duration are detailed in the above table. The temperatures are measured at the component to printed circuit board connections.

In process zone P1, the PC board and component pins are heated to a temperature of 150 °C to activate the flux in the solder paste. The temperature ramp up rate, R1, is limited to 3 °C per second to allow for even heating of both the PC board and component pins.

Process zone P2 should be of sufficient time duration (100 to 180 seconds) to dry the solder paste. The temperature is raised to a level just below the liquidus point of the solder.

Process zone P3 is the solder reflow zone. In zone P3, the temperature is quickly raised above the liquidus point of

solder to 260 °C (500 °F) for optimum results. The dwell time above the liquidus point of solder should be between 60 and 120 seconds. This is to assure proper coalescing of the solder paste into liquid solder and the formation of good solder connections. Beyond the recommended dwell time the intermetallic growth within the solder connections becomes excessive, resulting in the formation of weak and unreliable connections. The temperature is then rapidly reduced to a point below the solidus temperature of the solder to allow the solder within the connections to freeze solid.

Process zone P4 is the cool down after solder freeze. The cool down rate, R5, from the liquidus point of the solder to 25 °C (77 °F) should not exceed 6 °C per second maximum. This limitation is necessary to allow the PC board and component pins to change dimensions evenly, putting minimal stresses on the component.

It is recommended to perform reflow soldering no more than twice.

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

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