ESP8685 Series

Datasheet

Ultra-Low-Power SoC with RISC-V Single-Core CPU

Supporting IEEE 802.11b/g/n (2.4 GHz Wi-Fi) and Bluetooth® 5 (LE)

2 MB or 4 MB flash in the 4×4 mm QFN package

Including:

ESP8685H2

ESP8685H4

Version 1.0

Espressif Systems

Product Overview

ESP8685 is an ultra-low-power and highly-integrated MCU-based SoC solution that supports 2.4 GHz Wi-Fi and Bluetooth® Low Energy (Bluetooth LE). The block diagram of ESP8685 is shown below.

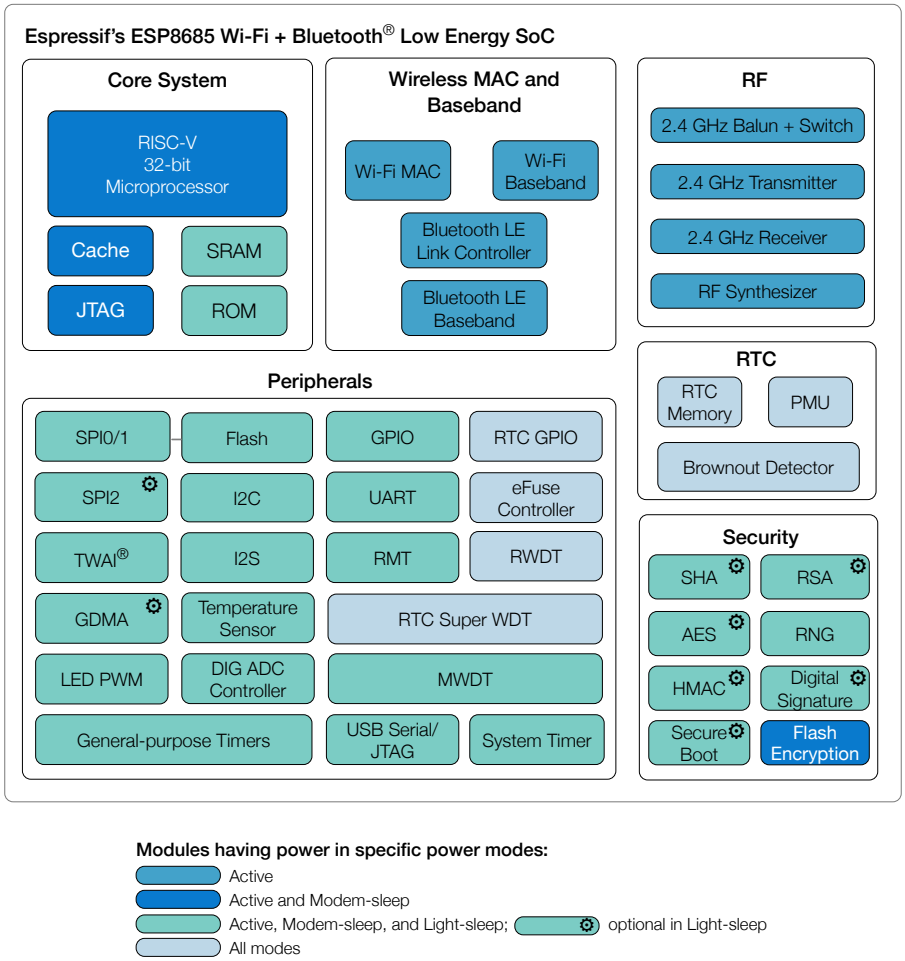

Figure 1: Block Diagram

Solution Highlights

- **A complete Wi-Fi subsystem** that complies with IEEE 802.11b/g/n protocol and supports Station mode, SoftAP mode, SoftAP + Station mode, and promiscuous mode
- **A Bluetooth LE subsystem** that supports features of Bluetooth 5 and Bluetooth mesh
- **State-of-the-art power and RF performance**
- **32-bit RISC-V single-core processor** with a four-stage pipeline that operates at up to 160 MHz
- **Storage capacities** ensured by 400 KB of SRAM (16 KB for cache) and 384 KB of ROM on the chip
- **Reliable security features** ensured by
  - Cryptographic hardware accelerators that support AES-128/256, Hash, RSA, HMAC, digital signature and secure boot
  - Random number generator
  - Permission control on accessing internal memory, external memory, and peripherals

  - External memory encryption and decryption
- **Rich set of peripheral interfaces and GPIOs**, ideal for various scenarios and complex applications

Features

Wi-Fi

- IEEE 802.11 b/g/n-compliant
- Supports 20 MHz, 40 MHz bandwidth in 2.4 GHz band
- 1T1R mode with data rate up to 150 Mbps
- Wi-Fi Multimedia (WMM)
- TX/RX A-MPDU, TX/RX A-MSDU
- Immediate Block ACK
- Fragmentation and defragmentation
- Transmit opportunity (TXOP)
- Automatic Beacon monitoring (hardware TSF)
- 4 × virtual Wi-Fi interfaces
- Simultaneous support for Infrastructure BSS in Station mode, SoftAP mode, Station + SoftAP mode, and promiscuous mode
  Note that when ESP8685 scans in Station mode, the SoftAP channel will change along with the Station channel
- Antenna diversity
- 802.11mc FTM
- Supports external power amplifier

Bluetooth

- Bluetooth LE: Bluetooth 5, Bluetooth mesh
- High power mode (18 dBm)
- Speed: 125 Kbps, 500 Kbps, 1 Mbps, 2 Mbps
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2
- Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna

CPU and Memory

- 32-bit RISC-V single-core processor, up to 160 MHz
- CoreMark® score:
  - 1 core at 160 MHz: 407.22 CoreMark; 2.55 CoreMark/MHz
- 384 KB ROM
- 400 KB SRAM (16 KB for cache)
- 8 KB SRAM in RTC
- SiP flash (see details in Chapter 1 *ESP8685 Series Comparison*)
- Access to flash accelerated by cache
- Supports flash in-Circuit Programming (ICP)

Advanced Peripheral Interfaces

- 15 × programmable GPIOs
- Digital interfaces:
  - 3 × SPI (SPI0 and SPI1 are used to connect the SiP flash. Only SPI2 is available)
  - 2 × UART
  - 1 × I2C
  - 1 × I2S
  - Remote control peripheral, with 2 transmit channels and 2 receive channels
  - LED PWM controller, with up to 6 channels
  - Full-speed USB Serial/JTAG controller
  - General DMA controller (GDMA), with 3 transmit channels and 3 receive channels
  - 1 × TWAI® controller compatible with ISO 11898-1 (CAN Specification 2.0)
- Analog interfaces:
  - 2 × 12-bit SAR ADCs, up to 6 channels
  - 1 × temperature sensor

- Timers:
  - 2 × 54-bit general-purpose timers
  - 3 × watchdog timers
  - 1 × 52-bit system timer

Low Power Management

- Power Management Unit with four power modes

Security

- Secure boot
- Flash encryption
- 4096-bit OTP, up to 1792 bits for use
- Cryptographic hardware acceleration:
  - AES-128/256 (FIPS PUB 197)
- Permission Control
- SHA Accelerator (FIPS PUB 180-4)
- RSA Accelerator
- Random Number Generator (RNG)
- HMAC
- Digital signature

Applications (A Non-exhaustive List)

With ultra-low power consumption, ESP8685 is an ideal choice for IoT devices in the following areas:

- Smart Home
  - Light control
  - Smart button
  - Smart plug
  - Indoor positioning
- Industrial Automation
  - Industrial robot
  - Mesh network
  - Human machine interface (HMI)
  - Industrial field bus
- Health Care
  - Health monitor
  - Baby monitor
- Consumer Electronics
  - Smart watch and bracelet
  - Over-the-top (OTT) devices
  - Wi-Fi speaker
  - Logger toys and proximity sensing toys
- Smart Agriculture
  - Smart greenhouse
  - Smart irrigation
  - Agriculture robot
- Retail and Catering
  - POS machines
  - Service robot
- Audio Device
  - Internet music players
  - Live streaming devices
  - Internet radio players
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers

Contents

List of Tables

List of Figures

1. ESP8685 Series Comparison

1.1 ESP8685 Series Nomenclature

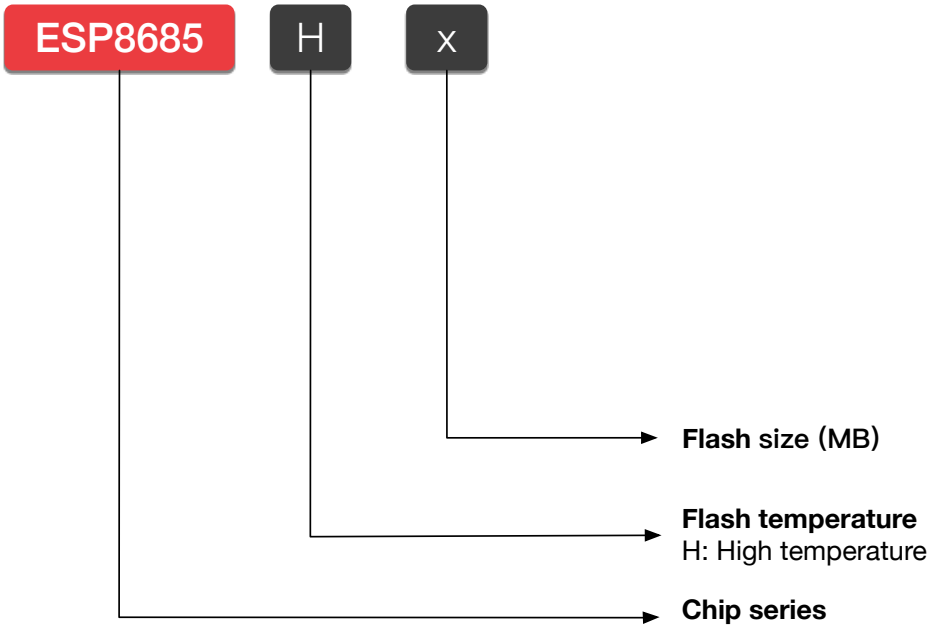

Figure 2: ESP8685 Series Nomenclature

1.2 Comparison

Table 1: ESP8685 Series Member Comparison

Ordering Code	SiP Flash	Ambient Temperature (°C)	Package (mm)
ESP8685H2	2 MB	–40 ~ 105	QFN28 (4*4)
ESP8685H4	4 MB	–40 ~ 105	QFN28 (4*4)

[1] SiP refers to flash integrated into the package.

2. Pin Definition

2.1 Pin Layout

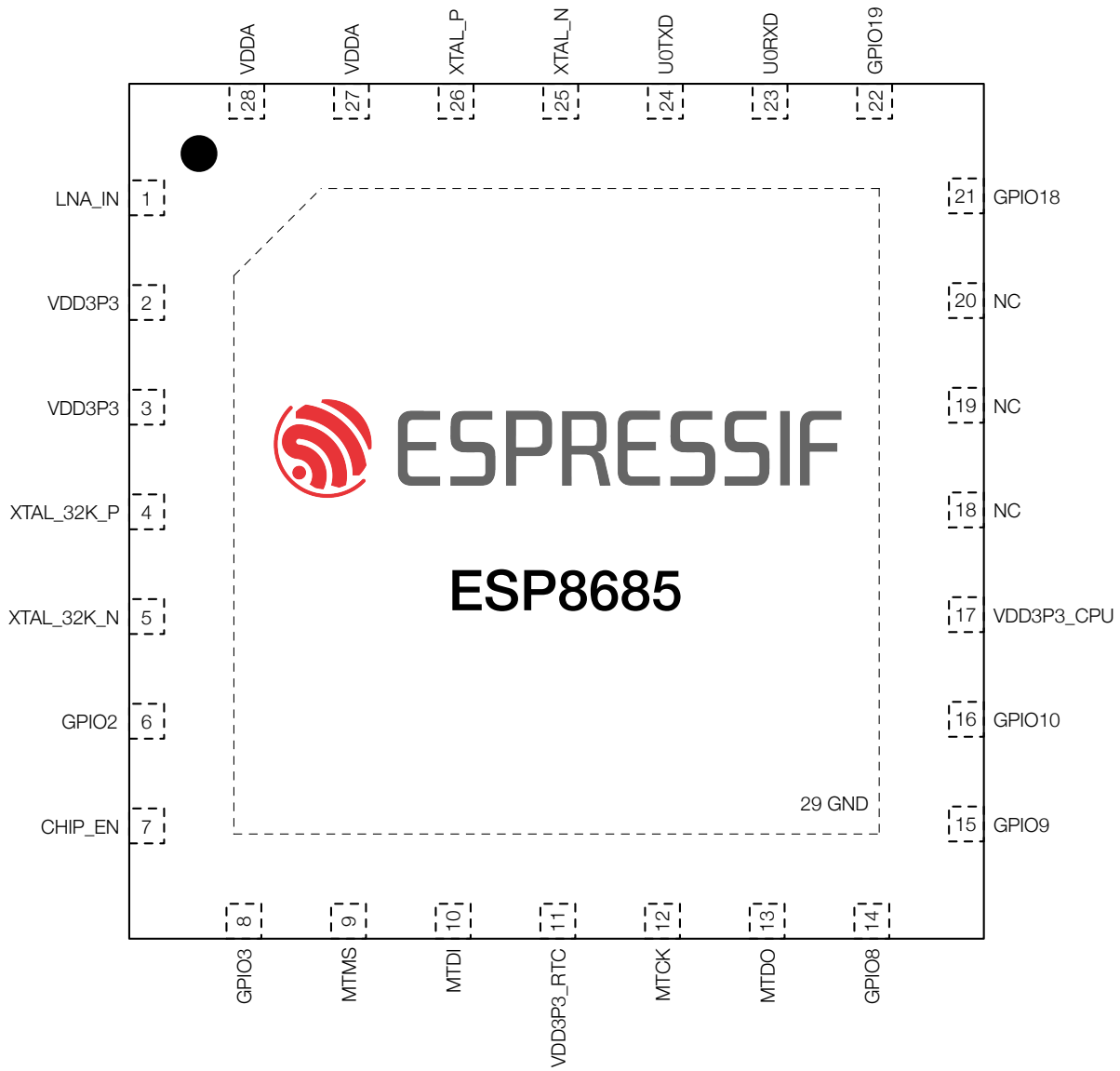

Figure 3: ESP8685H2 Pin Layout (Top View)

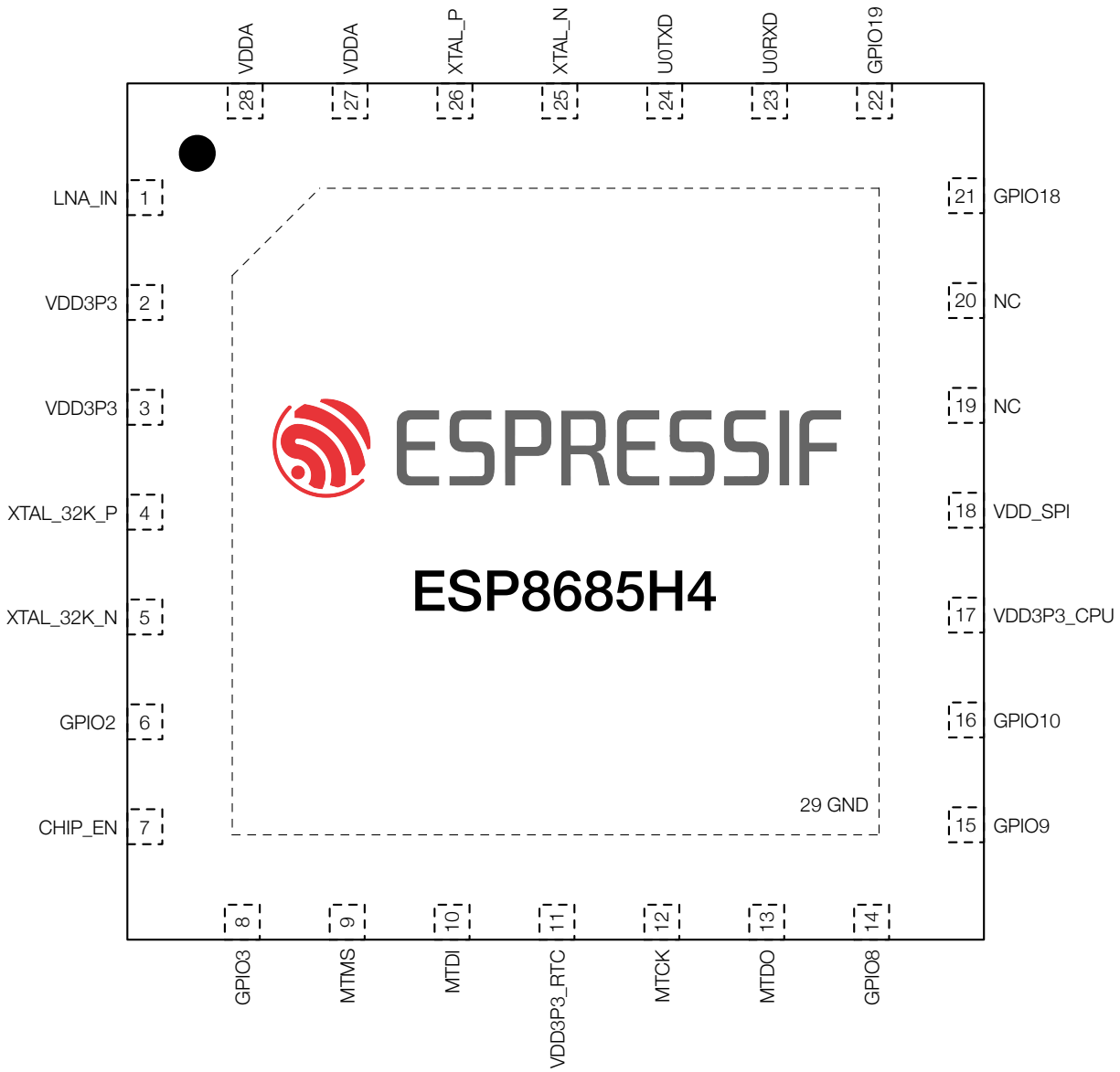

Figure 4: ESP8685H4 Pin Layout (Top View)

2.2 Pin Description

Table 2: ESP8685H2 Pin Description

Name	No.	Type	Power Domain	Function
LNA_IN	1	I/O	—	RF input and output
VDD3P3	2	P_A	—	Analog power supply
VDD3P3	3	P_A	—	Analog power supply
XTAL_32K_P	4	I/O/T	VDD3P3_RTC	GPIO0, ADC1_CH0, XTAL_32K_P
XTAL_32K_N	5	I/O/T	VDD3P3_RTC	GPIO1, ADC1_CH1, XTAL_32K_N
GPIO2	6	I/O/T	VDD3P3_RTC	GPIO2, ADC1_CH2, FSPIQ
CHIP_EN	7	I	VDD3P3_RTC	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the CHIP_EN pin floating.

Name	No.	Type	Power Domain	Function
GPIO3	8	I/O/T	VDD3P3_RTC	GPIO3, ADC1_CH3
MTMS	9	I/O/T	VDD3P3_RTC	GPIO4, ADC1_CH4, FSPIHD, MTMS
MTDI	10	I/O/T	VDD3P3_RTC	GPIO5, ADC2_CH0, FSPIWP MTDI
VDD3P3_RTC	11	P_D	—	Input power supply for RTC
MTCK	12	I/O/T	VDD3P3_CPU	GPIO6, FSPICLK, MTCK
MTDO	13	I/O/T	VDD3P3_CPU	GPIO7, FSPID, MTDO
GPIO8	14	I/O/T	VDD3P3_CPU	GPIO8
GPIO9	15	I/O/T	VDD3P3_CPU	GPIO9
GPIO10	16	I/O/T	VDD3P3_CPU	GPIO10, FSPICS0
VDD3P3_CPU	17	P_D	—	Input power supply for CPU IO
NC	18	—	—	NC
NC	19	—	—	NC
NC	20	—	—	NC
GPIO18	21	I/O/T	VDD3P3_CPU	GPIO18, USB_D-
GPIO19	22	I/O/T	VDD3P3_CPU	GPIO19, USB_D+
U0RXD	23	I/O/T	VDD3P3_CPU	GPIO20, U0RXD
U0TXD	24	I/O/T	VDD3P3_CPU	GPIO21, U0TXD
XTAL_N	25	—	—	External crystal output
XTAL_P	26	—	—	External crystal input
VDDA	27	P_A	—	Analog power supply
VDDA	28	P_A	—	Analog power supply
GND	29	G	—	Ground

[1] P_A: analog power supply; P_D: power supply for RTC IO; I: input; O: output; T: high impedance.

[2] The pin function in this table refers only to some fixed settings and do not cover all cases for signals that can be input and output through the GPIO matrix. For more information on the GPIO matrix, please refer to Table 9.

Table 3: ESP8685H4 Pin Description

Name	No.	Type	Power Domain	Function
LNA_IN	1	I/O	—	RF input and output
VDD3P3	2	P_A	—	Analog power supply
VDD3P3	3	P_A	—	Analog power supply
XTAL_32K_P	4	I/O/T	VDD3P3_RTC	GPIO0, ADC1_CH0, XTAL_32K_P
XTAL_32K_N	5	I/O/T	VDD3P3_RTC	GPIO1, ADC1_CH1, XTAL_32K_N
GPIO2	6	I/O/T	VDD3P3_RTC	GPIO2, ADC1_CH2, FSPIQ
CHIP_EN	7	I	VDD3P3_RTC	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the CHIP_EN pin floating.
GPIO3	8	I/O/T	VDD3P3_RTC	GPIO3, ADC1_CH3
MTMS	9	I/O/T	VDD3P3_RTC	GPIO4, ADC1_CH4, FSPIHD, MTMS
MTDI	10	I/O/T	VDD3P3_RTC	GPIO5, ADC2_CH0, FSPIWP MTDI
VDD3P3_RTC	11	P_D	—	Input power supply for RTC
MTCK	12	I/O/T	VDD3P3_CPU	GPIO6, FSPICLK, MTCK

Name	No.	Type	Power Domain	Function
MTDO	13	I/O/T	VDD3P3_CPU	GPIO7, FSPID, MTDO
GPIO8	14	I/O/T	VDD3P3_CPU	GPIO8
GPIO9	15	I/O/T	VDD3P3_CPU	GPIO9
GPIO10	16	I/O/T	VDD3P3_CPU	GPIO10, FSPICS0
VDD3P3_CPU	17	P_D	—	Input power supply for CPU IO
VDD_SPI	18	P_D	—	For internal use only
NC	19	—	—	NC
NC	20	—	—	NC
GPIO18	21	I/O/T	VDD3P3_CPU	GPIO18, USB_D-
GPIO19	22	I/O/T	VDD3P3_CPU	GPIO19, USB_D+
U0RXD	23	I/O/T	VDD3P3_CPU	GPIO20, U0RXD
U0TXD	24	I/O/T	VDD3P3_CPU	GPIO21, U0TXD
XTAL_N	25	—	—	External crystal output
XTAL_P	26	—	—	External crystal input
VDDA	27	P_A	—	Analog power supply
VDDA	28	P_A	—	Analog power supply
GND	29	G	—	Ground

[1] P_A: analog power supply; P_D: power supply for RTC IO; I: input; O: output; T: high impedance.

[2] The pin function in this table refers only to some fixed settings and do not cover all cases for signals that can be input and output through the GPIO matrix. For more information on the GPIO matrix, please refer to Table 9.

2.3 Power Scheme

ESP8685 has four input power pins:

- VDDA1
- VDDA2
- VDD3P3_RTC
- VDD3P3_CPU

VDDA1 and VDDA2 are the input power supply for the analog domain.

RTC IO is powered from VDD3P3_RTC.

The RTC domain is powered from Low Power Voltage Regulator, which is powered from VDD3P3_RTC.

The Digital System domain is powered from Digital System Voltage Regulator, which is powered from VDD3P3_CPU and VDD3P3_RTC at the same time.

Digital IO is powered from VDD3P3_CPU.

The power scheme diagram is shown in Figure 5.

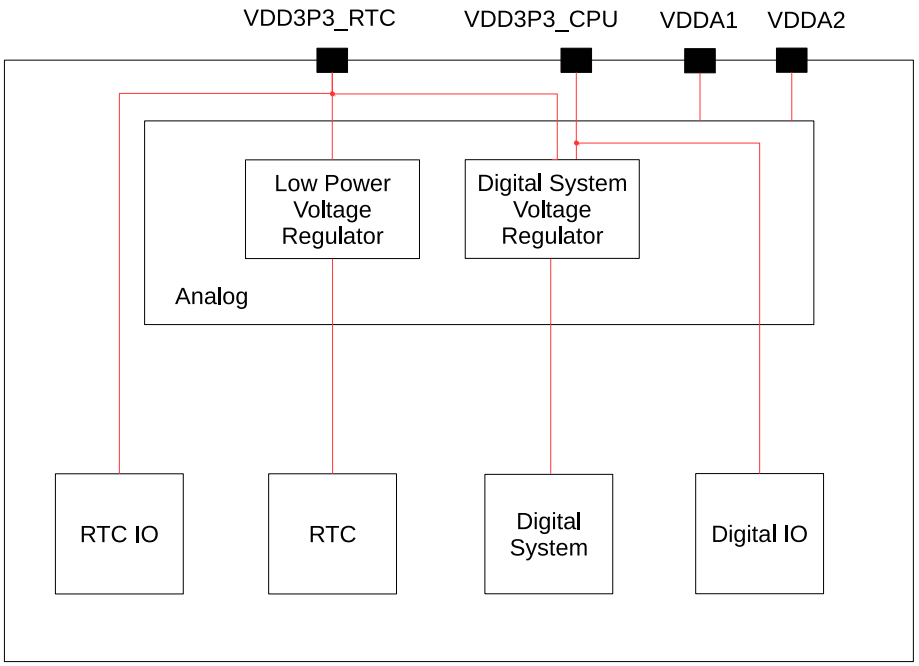

Figure 5: ESP8685 Power Scheme

Notes on CHIP_EN:

Figure 6 shows the power-up and reset timing of ESP8685. Details about the parameters are listed in Table 4.

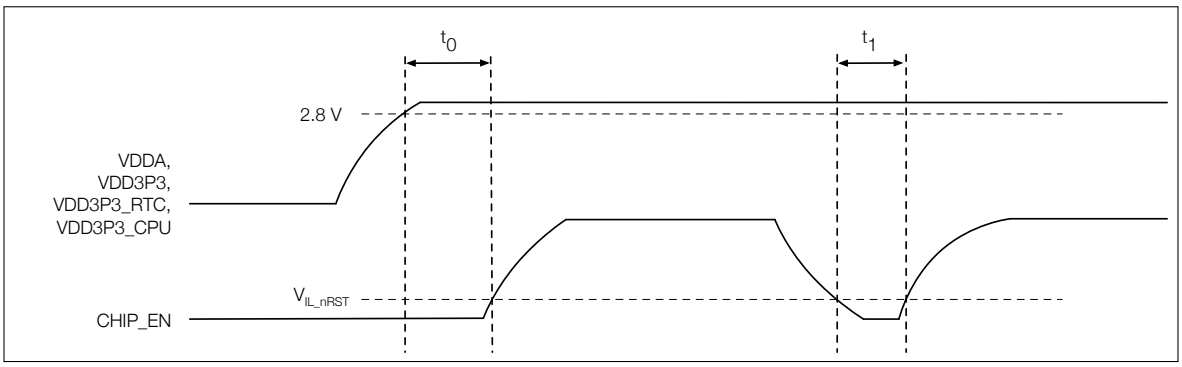

Figure 6: ESP8685 Power-up and Reset Timing

Table 4: Description of ESP8685 Power-up and Reset Timing Parameters

Parameter	Description	Min (μs)
t_0	Time between bringing up the VDDA, VDD3P3, VDD3P3_RTC, and VDD3P3_CPU rails, and activating CHIP_EN	50
t_1	Duration of CHIP_EN signal level < V_{IL_nRST} (refer to its value in Table 13) to reset the chip	50

2.4 Strapping Pins

ESP8685 series has three strapping pins:

- GPIO2
- GPIO8
- GPIO9

Software can read the values of GPIO2, GPIO8 and GPIO9 from GPIO_STRAPPING field in GPIO_STRAP_REG register.

During the chip's system reset, the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down.

Types of system reset include:

- power-on reset
- RTC watchdog reset
- brownout reset
- analog super watchdog reset
- crystal clock glitch detection reset

By default, GPIO9 is connected to the internal weak pull-up resistor. If GPIO9 is not connected or connected to an external high-impedance circuit, the latched bit value will be "1"

To change the strapping bit values, you can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP8685 series.

After reset, the strapping pins work as normal-function pins.

Table 5 lists detailed booting configurations of the strapping pins.

Table 5: Strapping Pins

Booting Mode [1]			
Pin	Default	SPI Boot	Download Boot
GPIO2	N/A	1	1
GPIO8	N/A	Don't care	1
GPIO9	Internal weak pull-up	1	0
Enabling/Disabling ROM Messages Print During Booting			
Pin	Default	Functionality	
GPIO8	N/A	When the value of eFuse field EFUSE_UART_PRINT_CONTROL is 0 (default), print is enabled and not controlled by GPIO8. 1, if GPIO8 is 0, print is enabled; if GPIO8 is 1, it is disabled. 2, if GPIO8 is 0, print is disabled; if GPIO8 is 1, it is enabled. 3, print is disabled and not controlled by GPIO8.	

[1] The strapping combination of GPIO8 = 0 and GPIO9 = 0 is invalid and will trigger unexpected behavior.

Figure 7 shows the setup and hold times for the strapping pins before and after the CHIP_EN signal goes high. Details about the parameters are listed in Table 6.

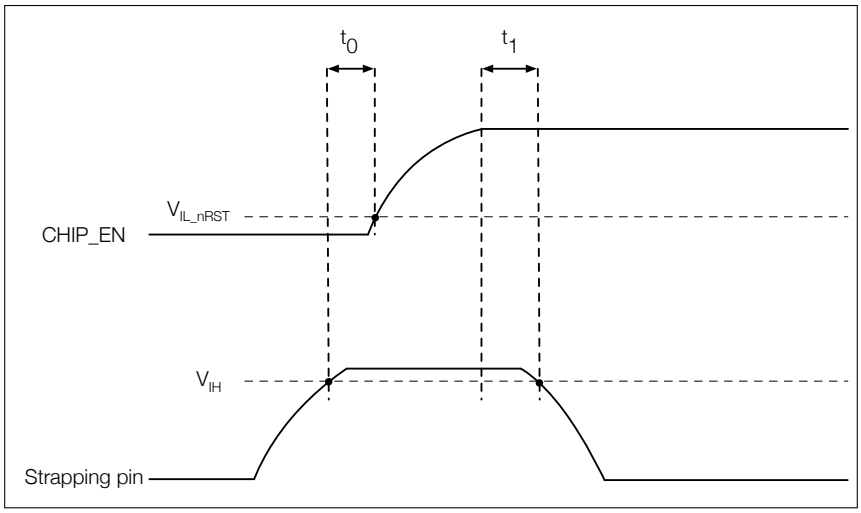

Figure 7: Setup and Hold Times for the Strapping Pins

Table 6: Parameter Descriptions of Setup and Hold Times for the Strapping Pins

Parameter	Description	Min (ms)
t_0	Setup time before CHIP_EN goes from low to high	0
t_1	Hold time after CHIP_EN goes high	3

3. Functional Description

This chapter describes the functions of ESP8685.

3.1 CPU and Memory

3.1.1 CPU

ESP8685 has a low-power 32-bit RISC-V single-core microprocessor with the following features:

- four-stage pipeline that supports a clock frequency of up to 160 MHz
- RV32IMC ISA
- 32-bit multiplier and 32-bit divider
- up to 32 vectored interrupts at seven priority levels
- up to 8 hardware breakpoints/watchpoints
- up to 16 PMP regions
- JTAG for debugging

3.1.2 Internal Memory

ESP8685's internal memory includes:

- **384 KB of ROM**: for booting and core functions.
- **400 KB of on-chip SRAM**: for data and instructions, running at a configurable frequency of up to 160 MHz. Of the 400 KB SRAM, 16 KB is configured for cache.
- **RTC FAST memory**: 8 KB of SRAM that can be accessed by the main CPU. It can retain data in Deep-sleep mode.
- **4 Kbit of eFuse**: 1792 bits are reserved for your data, such as encryption key and device ID.
- **SiP flash** : See details in Chapter 1 *ESP8685 Series Comparison*.

3.1.3 Address Mapping Structure

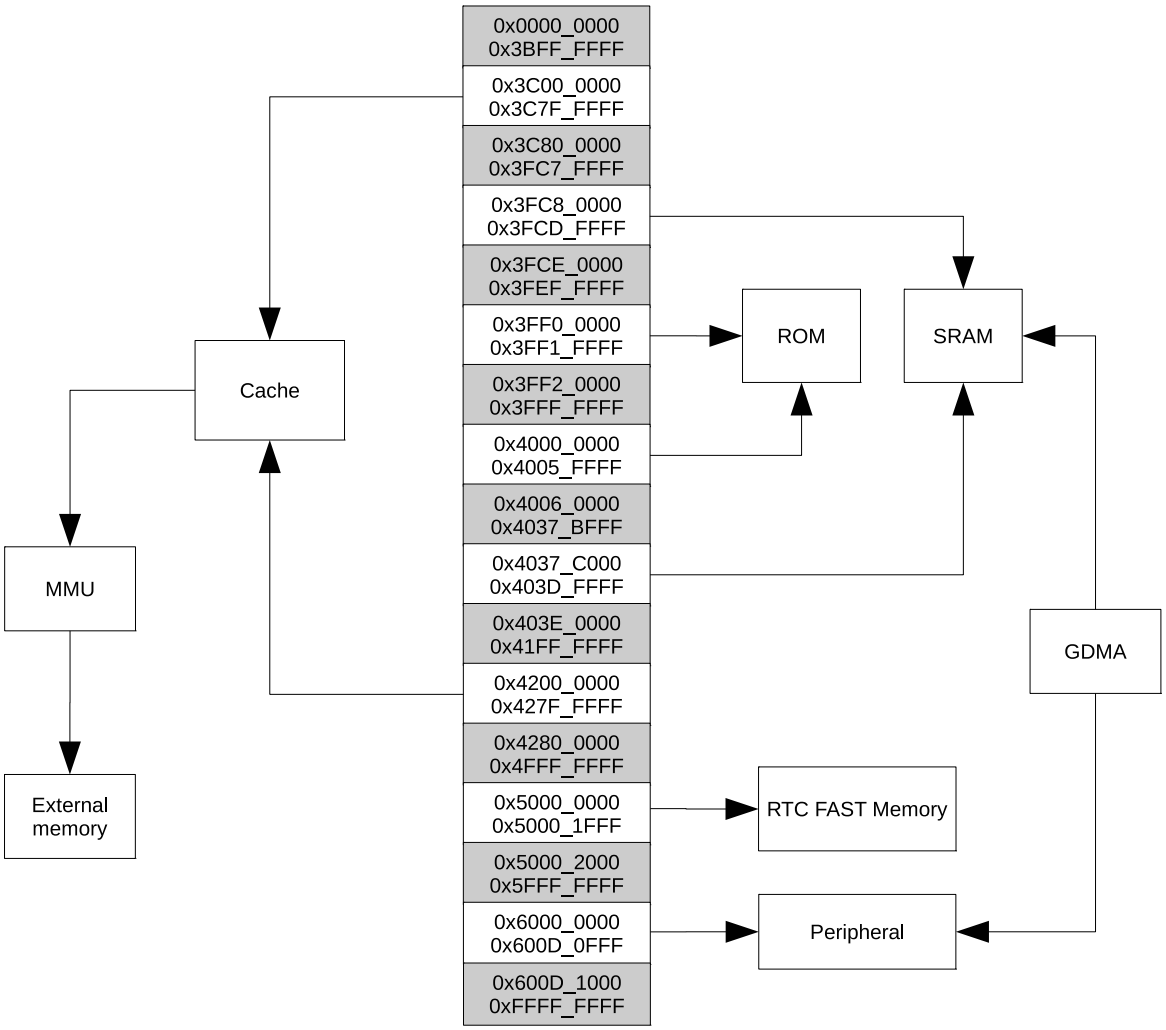

Figure 8: Address Mapping Structure

Note:
The memory space with gray background is not available for use.

3.1.4 Cache

ESP8685 has an eight-way set associative cache. This cache is read-only and has the following features:

- size: 16 KB
- block size: 32 bytes
- pre-load function
- lock function
- critical word first and early restart

3.2 System Clocks

3.2.1 CPU Clock

The CPU clock has three possible sources:

- external main crystal clock
- fast RC oscillator (typically about 17.5 MHz, and adjustable)
- PLL clock

The application can select the clock source from the three clocks above. The selected clock source drives the CPU clock directly, or after division, depending on the application. Once the CPU is reset, the default clock source would be the external main crystal clock divided by 2.

Note:
ESP32-C3 is unable to operate without an external main crystal clock.

3.2.2 RTC Clock

The RTC slow clock is used for RTC counter, RTC watchdog and low-power controller. It has three possible sources:

- external low-speed (32 kHz) crystal clock
- internal slow RC oscillator (typically about 136 kHz, and adjustable)
- internal fast RC oscillator divided clock (derived from the fast RC oscillator divided by 256)

The RTC fast clock is used for RTC peripherals and sensor controllers. It has two possible sources:

- external main crystal clock divided by 2
- internal fast RC oscillator divide-by-N clock (typically about 17.5 MHz, and adjustable)

3.3 Analog Peripherals

3.3.1 Analog-to-Digital Converter (ADC)

ESP8685 integrates two 12-bit SAR ADCs.

- ADC1 supports measurements on 5 channels, and is factory-calibrated.
- ADC2 supports measurements on 1 channel, and is not factory-calibrated.

For ADC characteristics, please refer to Table 14.

3.3.2 Temperature Sensor

The temperature sensor generates a voltage that varies with temperature. The voltage is internally converted via an ADC into a digital value.

The temperature sensor has a range of –40 °C to 125 °C. It is designed primarily to sense the temperature changes inside the chip. The temperature value depends on factors like microcontroller clock frequency or I/O load. Generally, the chip's internal temperature is higher than the operating ambient temperature.

3.4 Digital Peripherals

3.4.1 General Purpose Input / Output Interface (GPIO)

ESP8685 has 15 GPIO pins which can be assigned various functions by configuring corresponding registers. Besides digital signals, some GPIOs can be also used for analog functions, such as ADC.

All GPIOs have selectable internal pull-up or pull-down, or can be set to high impedance. When these GPIOs are configured as an input, the input value can be read by software through the register. Input GPIOs can also be set to generate edge-triggered or level-triggered CPU interrupts. All digital IO pins are bi-directional, non-inverting and tristate, including input and output buffers with tristate control. These pins can be multiplexed with other functions, such as the UART, etc. For low-power operations, the GPIOs can be set to holding state.

The IO MUX and the GPIO matrix are used to route signals from peripherals to GPIO pins. Together they provide highly configurable I/O. Using GPIO Matrix, peripheral input signals can be configured from any IO pins while peripheral output signals can be configured to any IO pins.

Table 7 shows the IO MUX functions of each pin.

Table 7: IO MUX Pin Functions

Name	No.	Function 0	Function 1	Function 2	Reset	Notes
XTAL_32K_P	4	GPIO0	GPIO0	—	0	R
XTAL_32K_N	5	GPIO1	GPIO1	—	0	R
GPIO2	6	GPIO2	GPIO2	FSPIQ	1	R
GPIO3	8	GPIO3	GPIO3	—	1	R
MTMS	9	MTMS	GPIO4	FSPIHD	1	R
MTDI	10	MTDI	GPIO5	FSPIWP	1	R
MTCK	12	MTCK	GPIO6	FSPICLK	1*	G
MTDO	13	MTDO	GPIO7	FSPID	1	G
GPIO8	14	GPIO8	GPIO8	—	1	—
GPIO9	15	GPIO9	GPIO9	—	3	—
GPIO10	16	GPIO10	GPIO10	FSPICS0	1	G
GPIO18	21	GPIO18	GPIO18	—	0	USB, G
GPIO19	22	GPIO19	GPIO19	—	0*	USB
U0RXD	23	U0RXD	GPIO20	—	3	G
U0TXD	24	U0TXD	GPIO21	—	4	—

Reset

The default configuration of each pin after reset:

- **0** - input disabled, in high impedance state (IE = 0)
- **1** - input enabled, in high impedance state (IE = 1)
- **2** - input enabled, pull-down resistor enabled (IE = 1, WPD = 1)
- **3** - input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
- **4** - output enabled, pull-up resistor enabled (OE = 1, WPU = 1)
- **0*** - input disabled, pull-up resistor enabled (IE = 0, WPU = 0, USB_WPU = 1). See details in Notes
- **1*** - When the value of eFuse bit EFUSE_DIS_PAD_JTAG is

0, input enabled, pull-up resistor enabled (IE = 1, WPU = 1)
1, input enabled, in high impedance state (IE = 1)

We recommend pulling high or low GPIO pins in high impedance state to avoid unnecessary power consumption. You may add pull-up and pull-down resistors in your PCB design referring to Table 13, or enable internal pull-up and pull-down resistors during software initialization.

Notes

- **R** - These pins have analog functions.
- **USB** - GPIO18 and GPIO19 are USB pins. The pull-up value of a USB pin is controlled by the pin's pull-up value together with USB pull-up value. If any of the two pull-up values is 1, the pin's pull-up resistor will be enabled. The pull-up resistors of USB pins are controlled by USB_SERIAL_JTAG_DP_PULLUP bit.
- **G** - These pins have glitches during power-up. See details in Table 8.

Table 8: Power-Up Glitches on Pins

Pin	Glitch[1]	Typical Time Period (ns)
MTCK	Low-level glitch	5
MTDO	Low-level glitch	5
GPIO10	Low-level glitch	5
U0RXD	Low-level glitch	5
GPIO18	Pull-up glitch	50000

[1] Low-level glitch: the pin is at a low level during the time period;
High-level glitch: the pin is at a high level during the time period;
Pull-up glitch: the pin is pulled up during the time period;
Pull-down glitch: the pin is pulled down during the time period.

Table 9 shows the peripheral input/output signals via GPIO matrix.

Please pay attention to the configuration of the bit GPIO_FUNC*n*_OEN_SEL:

- GPIO_FUNC*n*_OEN_SEL = 1: the output enable is controlled by the corresponding bit *n* of GPIO_ENABLE_REG:
  - GPIO_ENABLE_REG = 0: output is disabled;
  - GPIO_ENABLE_REG = 1: output is enabled;
- GPIO_FUNC*n*_OEN_SEL = 0: use the output enable signal from peripheral, for example SPIQ_oe in the column "Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0" of Table 9. Note that the signals such as SPIQ_oe can be 1 (1'd1) or 0 (1'd0), depending on the configuration of corresponding peripherals. If it is 1'd1 in the "Output enable signal when GPIO_FUNC*n*_OEN_SEL = 0", it indicates that once the register GPIO_FUNC*n*_OEN_SEL is cleared, the output signal is always enabled by default.

Note:
Signals are numbered consecutively, but not all signals are valid.
- For input signals, only 6 ~ 11, 45, 53, 54, 63 ~ 68, 97 ~ 100 are valid.
- For output signals, only 6 ~ 11, 45 ~ 50, 53 ~ 58, 63 ~ 73, 97 ~ 100, 123 ~ 125 are valid.

Table 9: Peripheral Signals via GPIO Matrix

Signal No.	Input Signal	Default value	Direct Input through IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL= 0	Direct Output through IO_MUX
0	-	-	-	-	1'd1	no
1	-	-	-	-	1'd1	no
2	-	-	-	-	1'd1	no
3	-	-	-	-	1'd1	no
4	-	-	-	-	1'd1	no
5	-	-	-	-	1'd1	no
6	U0RXD_in	0	yes	U0TXD_out	1'd1	yes
7	U0CTS_in	0	no	U0RTS_out	1'd1	no
8	U0DSR_in	0	no	U0DTR_out	1'd1	no
9	U1RXD_in	0	no	U1TXD_out	1'd1	no
10	U1CTS_in	0	no	U1RTS_out	1'd1	no
11	U1DSR_in	0	no	U1DTR_out	1'd1	no
12	I2S_MCLK_in	0	no	I2S_MCLK_out	1'd1	no
13	I2SO_BCK_in	0	no	I2SO_BCK_out	1'd1	no
14	I2SO_WS_in	0	no	I2SO_WS_out	1'd1	no
15	I2SI_SD_in	0	no	I2SO_SD_out	1'd1	no
16	I2SI_BCK_in	0	no	I2SI_BCK_out	1'd1	no
17	I2SI_WS_in	0	no	I2SI_WS_out	1'd1	no
18	gpio_bt_priority	0	no	gpio_wlan_prio	1'd1	no
19	gpio_bt_active	0	no	gpio_wlan_active	1'd1	no
20	-	-	-	-	1'd1	no
21	-	-	-	-	1'd1	no
22	-	-	-	-	1'd1	no
23	-	-	-	-	1'd1	no
24	-	-	-	-	1'd1	no

Signal No.	Input Signal	Default value	Direct Input through IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL= 0	Direct Output through IO_MUX
25	-	-	-	-	1'd1	no
26	-	-	-	-	1'd1	no
27	-	-	-	-	1'd1	no
28	cpu_gpio_in0	0	no	cpu_gpio_out0	cpu_gpio_out_oen0	no
29	cpu_gpio_in1	0	no	cpu_gpio_out1	cpu_gpio_out_oen1	no
30	cpu_gpio_in2	0	no	cpu_gpio_out2	cpu_gpio_out_oen2	no
31	cpu_gpio_in3	0	no	cpu_gpio_out3	cpu_gpio_out_oen3	no
32	cpu_gpio_in4	0	no	cpu_gpio_out4	cpu_gpio_out_oen4	no
33	cpu_gpio_in5	0	no	cpu_gpio_out5	cpu_gpio_out_oen5	no
34	cpu_gpio_in6	0	no	cpu_gpio_out6	cpu_gpio_out_oen6	no
35	cpu_gpio_in7	0	no	cpu_gpio_out7	cpu_gpio_out_oen7	no
36	-	-	-	usb_jtag_tck	1'd1	no
37	-	-	-	usb_jtag_tms	1'd1	no
38	-	-	-	usb_jtag_tdi	1'd1	no
39	-	-	-	usb_jtag_tdo	1'd1	no
40	-	-	-	-	1'd1	no
41	-	-	-	-	1'd1	no
42	-	-	-	-	1'd1	no
43	-	-	-	-	1'd1	no
44	-	-	-	-	1'd1	no
45	ext_adc_start	0	no	ledc_ls_sig_out0	1'd1	no
46	-	-	-	ledc_ls_sig_out1	1'd1	no
47	-	-	-	ledc_ls_sig_out2	1'd1	no
48	-	-	-	ledc_ls_sig_out3	1'd1	no
49	-	-	-	ledc_ls_sig_out4	1'd1	no
50	-	-	-	ledc_ls_sig_out5	1'd1	no
51	rmt_sig_in0	0	no	rmt_sig_out0	1'd1	no

Signal No.	Input Signal	Default value	Direct Input through IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL= 0	Direct Output through IO_MUX
52	rmt_sig_in1	0	no	rmt_sig_out1	1'd1	no
53	I2CEXT0_SCL_in	1	no	I2CEXT0_SCL_out	I2CEXT0_SCL_oe	no
54	I2CEXT0_SDA_in	1	no	I2CEXT0_SDA_out	I2CEXT0_SDA_oe	no
55	-	-	-	gpio_sd0_out	1'd1	no
56	-	-	-	gpio_sd1_out	1'd1	no
57	-	-	-	gpio_sd2_out	1'd1	no
58	-	-	-	gpio_sd3_out	1'd1	no
59	-	-	-	I2SO_SD1_out	1'd1	no
60	-	-	-	-	1'd1	no
61	-	-	-	-	1'd1	no
62	-	-	-	-	1'd1	no
63	FSPICLK_in	0	yes	FSPICLK_out_mux	FSPICLK_oe	yes
64	FSPIQ_in	0	yes	FSPIQ_out	FSPIQ_oe	yes
65	FSPID_in	0	yes	FSPID_out	FSPID_oe	yes
66	FSPIHD_in	0	yes	FSPIHD_out	FSPIHD_oe	yes
67	FSPIWP_in	0	yes	FSPIWP_out	FSPIWP_oe	yes
68	FSPICS0_in	0	yes	FSPICS0_out	FSPICS0_oe	yes
69	-	-	-	FSPICS1_out	FSPICS1_oe	no
70	-	-	-	FSPICS2_out	FSPICS2_oe	no
71	-	-	-	FSPICS3_out	FSPICS3_oe	no
72	-	-	-	FSPICS4_out	FSPICS4_oe	no
73	-	-	-	FSPICS5_out	FSPICS5_oe	no
74	twai_rx	1	no	twai_tx	1'd1	no
75	-	-	-	twai_bus_off_on	1'd1	no
76	-	-	-	twai_clkout	1'd1	no
77	-	-	-	-	1'd1	no
78	-	-	-	-	1'd1	no

Signal No.	Input Signal	Default value	Direct Input through IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL= 0	Direct Output through IO_MUX
79	-	-	-	-	1'd1	no
80	-	-	-	-	1'd1	no
81	-	-	-	-	1'd1	no
82	-	-	-	-	1'd1	no
83	-	-	-	-	1'd1	no
84	-	-	-	-	1'd1	no
85	-	-	-	-	1'd1	no
86	-	-	-	-	1'd1	no
87	-	-	-	-	1'd1	no
88	-	-	-	-	1'd1	no
89	-	-	-	ant_sel0	1'd1	no
90	-	-	-	ant_sel1	1'd1	no
91	-	-	-	ant_sel2	1'd1	no
92	-	-	-	ant_sel3	1'd1	no
93	-	-	-	ant_sel4	1'd1	no
94	-	-	-	ant_sel5	1'd1	no
95	-	-	-	ant_sel6	1'd1	no
96	-	-	-	ant_sel7	1'd1	no
97	sig_in_func_97	0	no	sig_in_func97	1'd1	no
98	sig_in_func_98	0	no	sig_in_func98	1'd1	no
99	sig_in_func_99	0	no	sig_in_func99	1'd1	no
100	sig_in_func_100	0	no	sig_in_func100	1'd1	no
101	-	-	-	-	1'd1	no
102	-	-	-	-	1'd1	no
103	-	-	-	-	1'd1	no
104	-	-	-	-	1'd1	no
105	-	-	-	-	1'd1	no

Signal No.	Input Signal	Default value	Direct Input through IO MUX	Output Signal	Output enable signal when GPIO_FUNC*n*_OEN_SEL= 0	Direct Output through IO_MUX
106	-	-	-	-	1'd1	no
107	-	-	-	-	1'd1	no
108	-	-	-	-	1'd1	no
109	-	-	-	-	1'd1	no
110	-	-	-	-	1'd1	no
111	-	-	-	-	1'd1	no
112	-	-	-	-	1'd1	no
113	-	-	-	-	1'd1	no
114	-	-	-	-	1'd1	no
115	-	-	-	-	1'd1	no
116	-	-	-	-	1'd1	no
117	-	-	-	-	1'd1	no
118	-	-	-	-	1'd1	no
119	-	-	-	-	1'd1	no
120	-	-	-	-	1'd1	no
121	-	-	-	-	1'd1	no
122	-	-	-	-	1'd1	no
123	-	-	-	CLK_OUT_out1	1'd1	no
124	-	-	-	CLK_OUT_out2	1'd1	no
125	-	-	-	CLK_OUT_out3	1'd1	no
126	-	-	-	-	1'd1	no
127	-	-	-	usb_jtag_trst	1'd1	no

3.4.2 Serial Peripheral Interface (SPI)

ESP8685 features three SPI interfaces (SPI0, SPI1, and SPI2). SPI0 and SPI1 can be configured to operate in SPI memory mode, while SPI2 can be configured to operate in general-purpose SPI modes.

- **SPI Memory mode**

  In SPI memory mode, SPI0 and SPI1 are used to connect the SiP flash in chip package. Data is transferred in bytes. Up to four-line SDR reads and writes are supported. The clock frequency is configurable to a maximum of 120 MHz.

- **SPI2 General-purpose SPI (GP-SPI) mode**

  When SPI2 acts as a general-purpose SPI, it can operate in master and slave modes. SPI2 supports two-line full-duplex communication and single-/two-/four-line half-duplex communication in both master and slave modes. The host's clock frequency is configurable. Data is transferred in bytes. The clock polarity (CPOL) and phase (CPHA) are also configurable. The SPI2 interface can connect to GDMA.

  - In master mode, the clock frequency is 80 MHz at most, and the four modes of SPI transfer format are supported.
  - In slave mode, the clock frequency is 60 MHz at most, and the four modes of SPI transfer format are also supported.

3.4.3 Universal Asynchronous Receiver Transmitter (UART)

ESP8685 has two UART interfaces, i.e. UART0 and UART1, which support IrDA and asynchronous communication (RS232 and RS485) at a speed of up to 5 Mbps. The UART controller provides hardware flow control (CTS and RTS signals) and software flow control (XON and XOFF). Both UART interfaces connect to GDMA via UHCI0, and can be accessed by the GDMA controller or directly by the CPU.

3.4.4 I2C Interface

ESP8685 has an I2C bus interface which is used for I2C master mode or slave mode, depending on your configuration. The I2C interface supports:

- standard mode (100 Kbit/s)
- fast mode (400 Kbit/s)
- up to 800 Kbit/s (constrained by SCL and SDA pull-up strength)
- 7-bit and 10-bit addressing mode
- double addressing mode
- 7-bit broadcast address

You can configure instruction registers to control the I2C interface for more flexibility.

3.4.5 I2S Interface

ESP8685 includes a standard I2S interface. This interface can operate as a master or a slave in full-duplex mode or half-duplex mode, and can be configured for 8-bit, 16-bit, 24-bit, or 32-bit serial communication. BCK clock frequency, from 10 kHz up to 40 MHz, is supported.

The I2S interface supports TDM PCM, TDM MSB alignment, TDM LSB alignment, TDM Phillips, and PDM TX interface. It connects to the GDMA controller.

3.4.6 Remote Control Peripheral

The Remote Control Peripheral (RMT) supports two channels of infrared remote transmission and two channels of infrared remote reception. By controlling pulse waveform through software, it supports various infrared and other single wire protocols. All four channels share a 192 × 32-bit memory block to store transmit or receive waveform.

3.4.7 LED PWM Controller

The LED PWM controller can generate independent digital waveform on six channels. The LED PWM controller:

- can generate digital waveform with configurable periods and duty cycle. The accuracy of duty cycle can be up to 18 bits.
- has multiple clock sources, including APB clock and external main crystal clock.
- can operate when the CPU is in Light-sleep mode.
- supports gradual increase or decrease of duty cycle, which is useful for the LED RGB color-gradient generator.

3.4.8 General DMA Controller

ESP8685 has a general DMA controller (GDMA) with six independent channels, i.e. three transmit channels and three receive channels. These six channels are shared by peripherals with DMA feature. The GDMA controller implements a fixed-priority scheme among these channels, whose priority can be configured.

The GDMA controller controls data transfer using linked lists. It allows peripheral-to-memory and memory-to-memory data transfer at a high speed. All channels can access internal RAM.

Peripherals on ESP8685 with DMA feature are SPI2, UHCI0, I2S, AES, SHA, and ADC.

3.4.9 USB Serial/JTAG Controller

ESP8685 integrates a USB Serial/JTAG controller. This controller has the following features:

- CDC-ACM virtual serial port and JTAG adapter functionality
- USB 2.0 full speed compliant, capable of up to 12 Mbit/s transfer speed (Note that this controller does not support the faster 480 Mbit/s high-speed transfer mode)
- programming SiP flash
- CPU debugging with compact JTAG instructions
- a full-speed USB PHY integrated in the chip

3.4.10 TWAI® Controller

ESP8685 has a TWAI® controller with the following features:

- compatible with ISO 11898-1 protocol (CAN Specification 2.0)
- standard frame format (11-bit ID) and extended frame format (29-bit ID)
- bit rates from 1 Kbit/s to 1 Mbit/s
- multiple modes of operation: Normal, Listen Only, and Self-Test (no acknowledgment required)
- 64-byte receive FIFO

- acceptance filter (single and dual filter modes)
- error detection and handling: error counters, configurable error interrupt threshold, error code capture, arbitration lost capture

3.5 Radio and Wi-Fi

ESP8685 radio consists of the following blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- bias and regulators
- balun and transmit-receive switch
- clock generator

3.5.1 2.4 GHz Receiver

The 2.4 GHz receiver demodulates the 2.4 GHz RF signal to quadrature baseband signals and converts them to the digital domain with two high-resolution, high-speed ADCs. To adapt to varying signal channel conditions, ESP8685 integrates RF filters, Automatic Gain Control (AGC), DC offset cancelation circuits, and baseband filters.

3.5.2 2.4 GHz Transmitter

The 2.4 GHz transmitter modulates the quadrature baseband signals to the 2.4 GHz RF signal, and drives the antenna with a high-powered CMOS power amplifier. The use of digital calibration further improves the linearity of the power amplifier.

Additional calibrations are integrated to cancel any radio imperfections, such as:

- carrier leakage
- I/Q amplitude/phase matching
- baseband nonlinearities
- RF nonlinearities
- antenna matching

These built-in calibration routines reduce the cost, time, and specialized equipment required for product testing.

3.5.3 Clock Generator

The clock generator produces quadrature clock signals of 2.4 GHz for both the receiver and the transmitter. All components of the clock generator are integrated into the chip, including inductors, varactors, filters, regulators and dividers.

The clock generator has built-in calibration and self-test circuits. Quadrature clock phases and phase noise are optimized on chip with patented calibration algorithms which ensure the best performance of the receiver and the transmitter.

3.5.4 Wi-Fi Radio and Baseband

ESP8685 Wi-Fi radio and baseband support the following features:

- 802.11b/g/n
- 802.11n MCS0-7 that supports 20 MHz and 40 MHz bandwidth
- 802.11n MCS32
- 802.11n 0.4 μs guard interval
- data rate up to 150 Mbps
- RX STBC (single spatial stream)
- adjustable transmitting power
- antenna diversity
  ESP8685 supports antenna diversity with an external RF switch. This switch is controlled by one or more GPIOs, and used to select the best antenna to minimize the effects of channel imperfections.

3.5.5 Wi-Fi MAC

ESP8685 implements the full 802.11 b/g/n Wi-Fi MAC protocol. It supports the Basic Service Set (BSS) STA and SoftAP operations under the Distributed Control Function (DCF). Power management is handled automatically with minimal host interaction to minimize the active duty period.

ESP8685 Wi-Fi MAC applies the following low-level protocol functions automatically:

- 4 × virtual Wi-Fi interfaces
- infrastructure BSS in Station mode, SoftAP mode, Station + SoftAP mode, and promiscuous mode
- RTS protection, CTS protection, Immediate Block ACK
- fragmentation and defragmentation
- TX/RX A-MPDU, TX/RX A-MSDU
- transmit opportunity (TXOP)
- Wi-Fi multimedia (WMM)
- GCMP, CCMP, TKIP, WAPI, WEP, BIP, WPA2-PSK/WPA2-Enterprise, and WPA3-PSK/WPA3-Enterprise
- automatic beacon monitoring (hardware TSF)
- 802.11mc FTM

3.5.6 Networking Features

Espressif provides libraries for TCP/IP networking, ESP-WIFI-MESH networking, and other networking protocols over Wi-Fi. TLS 1.0, 1.1 and 1.2 is also supported.

3.6 Bluetooth LE

ESP8685 includes a Bluetooth Low Energy subsystem that integrates a hardware link layer controller, an RF/modem block and a feature-rich software protocol stack. It supports the core features of Bluetooth 5 and Bluetooth mesh.

3.6.1 Bluetooth LE Radio and PHY

Bluetooth Low Energy radio and PHY in ESP8685 support:

- 1 Mbps PHY
- 2 Mbps PHY for higher data rates
- coded PHY for longer range (125 Kbps and 500 Kbps)
- listen before talk (LBT), implemented in hardware
- antenna diversity with an external RF switch
  This switch is controlled by one or more GPIOs, and used to select the best antenna to minimize the effects of channel imperfections.

3.6.2 Bluetooth LE Link Layer Controller

Bluetooth Low Energy Link Layer Controller in ESP8685 supports:

- LE advertising extensions, to enhance broadcasting capacity and broadcast more intelligent data
- multiple advertisement sets
- simultaneous advertising and scanning
- multiple connections in simultaneous central and peripheral roles
- adaptive frequency hopping and channel assessment
- LE channel selection algorithm #2
- connection parameter update
- high duty cycle non-connectable advertising
- LE privacy 1.2
- LE data packet length extension
- link layer extended scanner filter policies
- low duty cycle directed advertising
- link layer encryption
- LE Ping

3.7 Low Power Management

With the use of advanced power-management technologies, ESP8685 can switch between different power modes:

- Active mode: CPU and chip radio are powered on. The chip can receive, transmit, or listen.
- Modem-sleep mode: The CPU is operational and the clock speed can be reduced. Wi-Fi base band, Bluetooth LE base band, and radio are disabled, but Wi-Fi and Bluetooth LE connection can remain active.
- Light-sleep mode: The CPU is paused. Any wake-up events (MAC, host, RTC timer, or external interrupts) will wake up the chip. Wi-Fi and Bluetooth LE connection can remain active.
- Deep-sleep mode: CPU and most peripherals are powered down. Only the RTC memory is powered on. Wi-Fi connection data are stored in the RTC memory. The RTC timer or the RTC GPIOs can wake up the chip from the Deep-sleep mode.

For power consumption in different power modes, please refer to Table 16.

3.8 Timers

3.8.1 General Purpose Timers

ESP8685 is embedded with two 54-bit general-purpose timers, which are based on 16-bit prescalers and 54-bit auto-reload-capable up/down-timers.

The timers' features are summarized as follows:

- a 16-bit clock prescaler, from 1 to 65536
- a 54-bit time-base counter programmable to be incrementing or decrementing
- able to read real-time value of the time-base counter
- halting and resuming the time-base counter
- programmable alarm generation
- level interrupt generation

3.8.2 System Timer

ESP8685 integrates a 52-bit system timer, which has two 52-bit counters and three comparators. The system timer has the following features:

- counters with a fixed clock frequency of 16 MHz
- three types of independent interrupts generated according to alarm value
- two alarm modes: target mode and period mode
- 52-bit target alarm value and 26-bit periodic alarm value
- automatic reload of counter value
- counters can be stalled if the CPU is stalled or in OCD mode

3.8.3 Watchdog Timers

ESP8685 contains three watchdog timers: one in each of the two timer groups (called Main System Watchdog Timers, or MWDT) and one in the RTC module (called the RTC Watchdog Timer, or RWDT).

During the flash boot process, RWDT and the MWDT in timer group 0 (TIMG0) are enabled automatically in order to detect and recover from booting errors.

Watchdog timers have the following features:

- four stages, each with a programmable timeout value. Each stage can be configured, enabled and disabled separately
- interrupt, CPU reset, or core reset for MWDT upon expiry of each stage; interrupt, CPU reset, core reset, or system reset for RWDT upon expiry of each stage
- 32-bit expiry counter
- write protection, to prevent RWDT and MWDT configuration from being altered inadvertently
- flash boot protection
  If the boot process from an SPI flash does not complete within a predetermined period of time, the watchdog will reboot the entire main system.

3.9 Cryptographic Hardware Accelerators

ESP8685 is equipped with hardware accelerators of general algorithms, such as AES-128/AES-256 (FIPS PUB 197), ECB/CBC/OFB/CFB/CTR (NIST SP 800-38A), SHA1/SHA224/SHA256 (FIPS PUB 180-4), and RSA3072. The chip also supports independent arithmetic, such as Big Integer Multiplication and Big Integer Modular Multiplication. The maximum operation length for RSA and Big Integer Modular Multiplication is 3072 bits. The maximum factor length for Big Integer Multiplication is 1536 bits.

3.10 Physical Security Features

- Transparent flash encryption (AES-XTS algorithm) with software inaccessible key prevents unauthorized readout of your application code or data.
- Secure boot feature uses a hardware root of trust to ensure only signed firmware (with RSA-PSS signature) can be booted.
- HMAC module can use a software inaccessible MAC key to generate MAC signatures for identity verification and other purposes.
- Digital Signature module can use a software inaccessible secure key to generate RSA signatures for identity verification.
- World Controller provides two running environments for software. All hardware and software resources are sorted to two groups, and placed in either secure or general world. The secure world cannot be accessed by hardware in the general world, thus establishing a security boundary.

3.11 Peripheral Pin Configurations

Table 10: Peripheral Pin Configurations

Interface	Signal	Pin	Function
ADC	ADC1_CH0	XTAL_32K_P	Two 12-bit SAR ADCs
	ADC1_CH1	XTAL_32K_N	
	ADC1_CH2	GPIO2	
	ADC1_CH3	GPIO3	
	ADC1_CH4	MTMS	
	ADC2_CH0	MTDI	
JTAG	MTDI	MTDI	JTAG for software debugging
	MTCK	MTCK	
	MTMS	MTMS	
	MTDO	MTDO	
UART	U0RXD_in	Any GPIO pins	Two UART channels with hardware flow control and GDMA
	U0CTS_in		
	U0DSR_in		
	U0TXD_out		
	U0RTS_out		
	U0DTR_out		
	U1RXD_in		
	U1CTS_in		
	U1DSR_in		

Interface	Signal	Pin	Function
	U1TXD_out		
	U1RTS_out		
	U1DTR_out		
I2C	I2CEXT0_SCL_in	Any GPIO pins	One I2C channel in slave or master mode
	I2CEXT0_SDA_in		
	I2CEXT1_SCL_in		
	I2CEXT1_SDA_in		
	I2CEXT0_SCL_out		
	I2CEXT0_SDA_out		
	I2CEXT1_SCL_out		
	I2CEXT1_SDA_out		
LED PWM	ledc_ls_sig_out0~5	Any GPIO pins	Six independent PWM channels
I2S	I2S0O_BCK_in	Any GPIO pins	Stereo input and output from/to the audiocodec
	I2S_MCLK_in		
	I2SO_WS_in		
	I2SI_SD_in		
	I2SI_BCK_in		
	I2SI_WS_in		
	I2SO_BCK_out		
	I2S_MCLK_out		
	I2SO_WS_out		
	I2SO_SD_out		
	I2SI_BCK_out		
	I2SI_WS_out		
	I2SO_SD1_out		
SPI2	FSPICLK_in/_out_mux	Any GPIO pins	• Master mode and slave mode of SPI, Dual SPI, Quad SPI, and QPI • Four modes of SPI transfer format • Configurable SPI frequency • 64-byte FIFO or GDMA buffer
	FSPICS0_in/_out		
	FSPICS1~5_out		
	FSPID_in/_out		
	FSPIQ_in/_out		
	FSPIWP_in/_out		
	FSPIHD_in/_out		
Remote Control Peripheral	RMT_SIG_IN0~1	Any GPIO pins	Two channels for an IR transceiver of various waveforms
	RMT_SIG_OUT0~1		
USB Serial/JTAG	USB_D+	GPIO19	USB-to-serial converter, and USB-to-JTAG converter
	USB_D-	GPIO18	
TWAI	twai_rx	Any GPIO pins	Compatible with ISO 11898-1 protocol
	twai_tx		
	twai_bus_off_on		
	twai_clkout		

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses beyond the absolute maximum ratings listed in the table below may cause permanent damage to the device. These are stress ratings only, and do not refer to the functional operation of the device.

Table 11: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
VDDA, VDD3P3, VDD3P3_RTC, VDD3P3_CPU	Voltage applied to power supply pins per power domain	–0.3	3.6	V
T_{STORE}	Storage temperature	–40	150	°C

4.2 Recommended Operating Conditions

Table 12: Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDDA, VDD3P3 VDD3P3_RTC	Voltage applied to power supply pins per power domain	3.0	3.3	3.6	V
VDD3P3_CPU[2]	Voltage applied to power supply pin	3.0	3.3	3.6	V
I_{VDD}[3]	Current delivered by external power supply	0.5	—	—	A
T_A	Operating ambient temperature	–40	—	105	°C

[1] For more information, please refer to Section 2.3 *Power Scheme*.

[2] To write eFuse, VDD3P3_CPU should not be higher than 3.3 V.

[3] If you use a single power supply, the recommended output current is 500 mA or more.

4.3 DC Characteristics (3.3 V, 25 °C)

Table 13: DC Characteristics (3.3 V, 25 °C)

Symbol	Parameter	Min	Typ	Max	Unit
C_{IN}	Pin capacitance	—	2	—	pF
V_{IH}	High-level input voltage	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL}	Low-level input voltage	–0.3	—	0.25 × VDD[1]	V
I_{IH}	High-level input current	—	—	50	nA
I_{IL}	Low-level input current	—	—	50	nA
V_{OH}[2]	High-level output voltage	0.8 × VDD[1]	—	—	V
V_{OL}[2]	Low-level output voltage	—	—	0.1 × VDD[1]	V
I_{OH}	High-level source current (VDD[1]= 3.3 V, V_{OH} >= 2.64 V, PAD_DRIVER = 3)	—	40	—	mA
I_{OL}	Low-level sink current (VDD[1]= 3.3 V, V_{OL} = 0.495 V, PAD_DRIVER = 3)	—	28	—	mA
R_{PU}	Pull-up resistor	—	45	—	kΩ
R_{PD}	Pull-down resistor	—	45	—	kΩ

Cont'd on next page

Table 13 – cont'd from previous page

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH_nRST}	Chip reset release voltage	0.75 × VDD[1]	—	VDD[1]+ 0.3	V
V_{IL_nRST}	Chip reset voltage	–0.3	—	0.25 × VDD[1]	V

[1] VDD is the I/O voltage for a particular power domain of pins.

[2] V_{OH} and V_{OL} are measured using high-impedance load.

4.4 ADC Characteristics

Table 14: ADC Characteristics

Symbol	Parameter	Min	Max	Unit
DNL (Differential nonlinearity)[1]	ADC connected to an external 100 nF capacitor; DC signal input; ambient temperature at 25 °C; Wi-Fi off	–7	7	LSB
INL (Integral nonlinearity)		–12	12	LSB
Sampling rate	—	—	100	kSPS [2]
Effective Range	ATTEN0	0	750	mV
	ATTEN1	0	1050	mV
	ATTEN2	0	1300	mV
	ATTEN3	0	2500	mV

[1] To get better DNL results, you can sample multiple times and apply a filter, or calculate the average value.

[2] kSPS means kilo samples-per-second.

4.5 Current Consumption

The current consumption measurements are taken with a 3.3 V supply at 25 °C of ambient temperature at the RF port. All transmitters' measurements are based on a 100% duty cycle.

Table 15: Current Consumption Depending on RF Modes

Work mode	Description		Peak (mA)
Active (RF working)	TX	802.11b, 1 Mbps, @21 dBm	335
		802.11g, 54 Mbps, @19 dBm	285
		802.11n, HT20, MCS7, @18.5 dBm	276
		802.11n, HT40, MCS7, @18.5 dBm	278
	RX	802.11b/g/n, HT20	84
		802.11n, HT40	87

Table 16: Current Consumption Depending on Work Modes

Work mode	Description		Typ	Unit
Modem-sleep[1, 2]	The CPU is powered on[3]	160 MHz	20	mA
		80 MHz	15	mA
Light-sleep	—		130	μA

Deep-sleep	RTC timer + RTC memory	5	μA
Power off	CHIP_PU is set to low level, the chip is powered off	1	μA

[1] The current consumption figures in Modem-sleep mode are for cases where the CPU is powered on and the cache idle.

[2] When Wi-Fi is enabled, the chip switches between Active and Modem-sleep modes. Therefore, current consumption changes accordingly.

[3] In Modem-sleep mode, the CPU frequency changes automatically. The frequency depends on the CPU load and the peripherals used.

4.6 Reliability

Table 17: Reliability Qualifications

Test Item	Test Conditions	Test Standard
HTOL (High Temperature Operating Life)	125 °C, 1000 hours	JESD22-A108
ESD (Electro-Static Discharge Sensitivity)	HBM (Human Body Mode)[1] ± 2000 V	JS-001
	CDM (Charge Device Mode)[2] ± 1000 V	JS-002
Latch up	Current trigger ± 200 mA	JESD78
	Voltage trigger 1.5 × VDD_{max}	
Preconditioning	Bake 24 hours @125 °C Moisture soak (level 3: 192 hours @30 °C, 60% RH) IR reflow solder: 260 + 0 °C, 20 seconds, three times	J-STD-020, JESD47, JESD22-A113
TCT (Temperature Cycling Test)	–65 °C / 150 °C, 500 cycles	JESD22-A104
uHAST (Highly Accelerated Stress Test, unbiased)	130 °C, 85% RH, 96 hours	JESD22-A118
HTSL (High Temperature Storage Life)	150 °C, 1000 hours	JESD22-A103
LTSL (Low Temperature Storage Life)	– 40 °C, 1000 hours	JESD22-A119

[1] JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

[2] JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

4.7 Wi-Fi Radio

Table 18: Wi-Fi Frequency

Parameter	Min (MHz)	Typ (MHz)	Max (MHz)
Center frequency of operating channel	2412	—	2484

4.7.1 Wi-Fi RF Transmitter (TX) Specifications

Table 19: TX Power with Spectral Mask and EVM Meeting 802.11 Standards

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	21.0	—
802.11b, 11 Mbps	—	21.0	—
802.11g, 6 Mbps	—	21.0	—
802.11g, 54 Mbps	—	19.0	—
802.11n, HT20, MCS0	—	20.0	—
802.11n, HT20, MCS7	—	18.5	—
802.11n, HT40, MCS0	—	20.0	—
802.11n, HT40, MCS7	—	18.5	—

Table 20: TX EVM Test

Rate	Min (dB)	Typ (dB)	SL[1] (dB)
802.11b, 1 Mbps, @21 dBm	—	–24.5	–10
802.11b, 11 Mbps, @21 dBm	—	–24.5	–10
802.11g, 6 Mbps, @21 dBm	—	–21.0	–5
802.11g, 54 Mbps, @19 dBm	—	–27.0	–25
802.11n, HT20, MCS0, @20 dBm	—	–22.5	–5
802.11n, HT20, MCS7, @18.5 dBm	—	–28.5	–27
802.11n, HT40, MCS0, @20 dBm	—	–22.5	–5
802.11n, HT40, MCS7, @18.5 dBm	—	–28.5	–27

[1] SL stands for standard limit value.

4.7.2 Wi-Fi RF Receiver (RX) Specifications

Table 21: RX Sensitivity

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	–98.4	—
802.11b, 2 Mbps	—	–96.0	—
802.11b, 5.5 Mbps	—	–93.0	—
802.11b, 11 Mbps	—	–88.6	—
802.11g, 6 Mbps	—	–93.8	—
802.11g, 9 Mbps	—	–92.2	—
802.11g, 12 Mbps	—	–91.0	—
802.11g, 18 Mbps	—	–88.4	—
802.11g, 24 Mbps	—	–85.8	—
802.11g, 36 Mbps	—	–82.0	—

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Table 21 – cont'd from previous page

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11g, 48 Mbps	—	–78.0	—
802.11g, 54 Mbps	—	–76.6	—
802.11n, HT20, MCS0	—	–93.6	—
802.11n, HT20, MCS1	—	–90.8	—
802.11n, HT20, MCS2	—	–88.4	—
802.11n, HT20, MCS3	—	–85.0	—
802.11n, HT20, MCS4	—	–81.8	—
802.11n, HT20, MCS5	—	–77.8	—
802.11n, HT20, MCS6	—	–76.0	—
802.11n, HT20, MCS7	—	–74.8	—
802.11n, HT40, MCS0	—	–90.0	—
802.11n, HT40, MCS1	—	–88.0	—
802.11n, HT40, MCS2	—	–85.2	—
802.11n, HT40, MCS3	—	–82.0	—
802.11n, HT40, MCS4	—	–78.8	—
802.11n, HT40, MCS5	—	–74.6	—
802.11n, HT40, MCS6	—	–73.0	—
802.11n, HT40, MCS7	—	–71.4	—

Table 22: Maximum RX Level

Rate	Min (dBm)	Typ (dBm)	Max (dBm)
802.11b, 1 Mbps	—	5	—
802.11b, 11 Mbps	—	5	—
802.11g, 6 Mbps	—	5	—
802.11g, 54 Mbps	—	0	—
802.11n, HT20, MCS0	—	5	—
802.11n, HT20, MCS7	—	0	—
802.11n, HT40, MCS0	—	5	—
802.11n, HT40, MCS7	—	0	—

Table 23: RX Adjacent Channel Rejection

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11b, 1 Mbps	—	35	—
802.11b, 11 Mbps	—	35	—
802.11g, 6 Mbps	—	31	—
802.11g, 54 Mbps	—	20	—
802.11n, HT20, MCS0	—	31	—

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Table 23 – cont'd from previous page

Rate	Min (dB)	Typ (dB)	Max (dB)
802.11n, HT20, MCS7	—	16	—
802.11n, HT40, MCS0	—	25	—
802.11n, HT40, MCS7	—	11	—

4.8 Bluetooth LE Radio

Table 24: Bluetooth LE Frequency

Parameter	Min (MHz)	Typ (MHz)	Max (MHz)
Center frequency of operating channel	2402	—	2480

4.8.1 Bluetooth LE RF Transmitter (TX) Specifications

Table 25: Transmitter Characteristics - Bluetooth LE 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	–27.00	0	18.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\lvert f_n \rvert_{n=0,\,1,\,2,\,..k}$	—	17.00	—	kHz
	Max $\lvert f_0 - f_n \rvert$	—	1.75	—	kHz
	Max $\lvert f_n - f_{n-5} \rvert$	—	1.46	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	0.80	—	kHz
Modulation characteristics	$\Delta\, f1_{avg}$	—	250.00	—	kHz
	Min $\Delta\, f2_{max}$ (for at least 99.9% of all $\Delta\, f2_{max}$)	—	190.00	—	kHz
	$\Delta\, f2_{avg}/\Delta\, f1_{avg}$	—	0.83	—	—
In-band spurious emissions	± 2 MHz offset	—	–37.62	—	dBm
	± 3 MHz offset	—	–41.95	—	dBm
	> ± 3 MHz offset	—	–44.48	—	dBm

Table 26: Transmitter Characteristics - Bluetooth LE 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	–27.00	0	18.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\lvert f_n \rvert_{n=0,\,1,\,2,\,..k}$	—	20.80	—	kHz
	Max $\lvert f_0 - f_n \rvert$	—	1.30	—	kHz
	Max $\lvert f_n - f_{n-5} \rvert$	—	1.33	—	kHz
	$\lvert f_1 - f_0 \rvert$	—	0.70	—	kHz
Modulation characteristics	$\Delta\, f1_{avg}$	—	498.00	—	kHz

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Table 26 – cont'd from previous page

Parameter	Description	Min	Typ	Max	Unit
	Min $\Delta f2_{max}$ (for at least 99.9% of all $\Delta f2_{max}$)	—	430.00	—	kHz
	$\Delta f2_{avg}/\Delta f1_{avg}$	—	0.93	—	—
In-band spurious emissions	± 4 MHz offset	—	–43.55	—	dBm
	± 5 MHz offset	—	–45.26	—	dBm
	> ± 5 MHz offset	—	–45.26	—	dBm

Table 27: Transmitter Characteristics - Bluetooth LE 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	–27.00	0	18.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\lvert f_n \rvert_{n=0,\,1,\,2,\,..k}$	—	17.50	—	kHz
	Max $\lvert f_0 - f_n \rvert$	—	0.45	—	kHz
	$\lvert f_n - f_{n-3} \rvert$	—	0.70	—	kHz
	$\lvert f_0 - f_3 \rvert$	—	0.30	—	kHz
Modulation characteristics	$\Delta f1_{avg}$	—	250.00	—	kHz
	Min $\Delta f1_{max}$ (for at least 99.9% of all$\Delta f2_{max}$)	—	235.00	—	kHz
In-band spurious emissions	± 2 MHz offset	—	–37.90	—	dBm
	± 3 MHz offset	—	–41.00	—	dBm
	> ± 3 MHz offset	—	–42.50	—	dBm

Table 28: Transmitter Characteristics - Bluetooth LE 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
RF transmit power	RF power control range	–27.00	0	18.00	dBm
	Gain control step	—	3.00	—	dB
Carrier frequency offset and drift	Max $\lvert f_n \rvert_{n=0,\,1,\,2,\,..k}$	—	17.00	—	kHz
	Max $\lvert f_0 - f_n \rvert$	—	0.88	—	kHz
	$\lvert f_n - f_{n-3} \rvert$	—	1.00	—	kHz
	$\lvert f_0 - f_3 \rvert$	—	0.20	—	kHz
Modulation characteristics	$\Delta f2_{avg}$	—	208.00	—	kHz
	Min $\Delta f2_{max}$ (for at least 99.9% of all $\Delta f2_{max}$)	—	190.00	—	kHz
In-band spurious emissions	± 2 MHz offset	—	–37.90	—	dBm
	± 3 MHz offset	—	–41.30	—	dBm
	> ± 3 MHz offset	—	–42.80	—	dBm

4.8.2 Bluetooth LE RF Receiver (RX) Specifications

Table 29: Receiver Characteristics - Bluetooth LE 1 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–97	—	dBm
Maximum received signal @30.8% PER	—	—	5	—	dBm
Co-channel C/I	—	—	8	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–3	—	dB
	F = F0 – 1 MHz	—	–4	—	dB
	F = F0 + 2 MHz	—	–29	—	dB
	F = F0 – 2 MHz	—	–31	—	dB
	F = F0 + 3 MHz	—	–33	—	dB
	F = F0 – 3 MHz	—	–27	—	dB
	F $\geq$ F0 + 4 MHz	—	–29	—	dB
	F $\leq$ F0 – 4 MHz	—	–38	—	dB
Image frequency	—	—	–29	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–41	—	dB
	F = F_{image} – 1 MHz	—	–33	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	–5	—	dBm
	2003 MHz ~ 2399 MHz	—	–18	—	dBm
	2484 MHz ~ 2997 MHz	—	–15	—	dBm
	3000 MHz ~ 12.75 GHz	—	–5	—	dBm
Intermodulation	—	—	–30	—	dBm

Table 30: Receiver Characteristics - Bluetooth LE 2 Mbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–93	—	dBm
Maximum received signal @30.8% PER	—	—	3	—	dBm
Co-channel C/I	—	—	10	—	dB
Adjacent channel selectivity C/I	F = F0 + 2 MHz	—	–7	—	dB
	F = F0 – 2 MHz	—	–7	—	dB
	F = F0 + 4 MHz	—	–28	—	dB
	F = F0 – 4 MHz	—	–26	—	dB
	F = F0 + 6 MHz	—	–26	—	dB
	F = F0 – 6 MHz	—	–27	—	dB
	F $\geq$ F0 + 8 MHz	—	–29	—	dB
	F $\leq$ F0 – 8 MHz	—	–28	—	dB
Image frequency	—	—	–28	—	dB
Adjacent channel to image frequency	F = F_{image} + 2 MHz	—	–26	—	dB
	F = F_{image} – 2 MHz	—	–7	—	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	—	–5	—	dBm
	2003 MHz ~ 2399 MHz	—	–19	—	dBm
	2484 MHz ~ 2997 MHz	—	–16	—	dBm
	3000 MHz ~ 12.75 GHz	—	–5	—	dBm
Intermodulation	—	—	–29	—	dBm

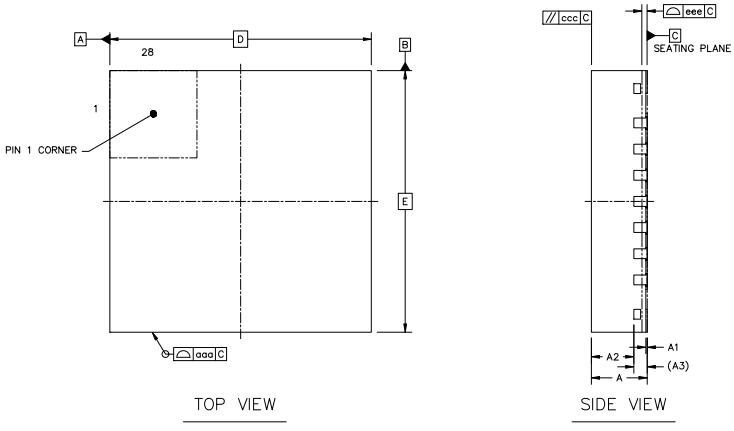
Table 31: Receiver Characteristics - Bluetooth LE 125 Kbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–105	—	dBm
Maximum received signal @30.8% PER	—	—	5	—	dBm
Co-channel C/I	—	—	3	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–6	—	dB
	F = F0 – 1 MHz	—	–6	—	dB
	F = F0 + 2 MHz	—	–33	—	dB
	F = F0 – 2 MHz	—	–43	—	dB
	F = F0 + 3 MHz	—	–37	—	dB
	F = F0 – 3 MHz	—	–47	—	dB
	F $\geq$ F0 + 4 MHz	—	–40	—	dB
	F $\leq$ F0 – 4 MHz	—	–50	—	dB
Image frequency	—	—	–40	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–50	—	dB
	F = F_{image} – 1 MHz	—	–37	—	dB

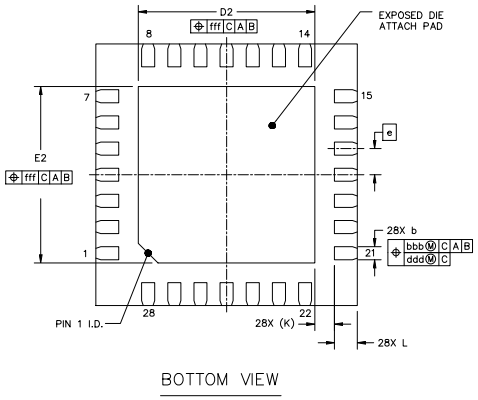
Table 32: Receiver Characteristics - Bluetooth LE 500 Kbps

Parameter	Description	Min	Typ	Max	Unit
Sensitivity @30.8% PER	—	—	–100	—	dBm
Maximum received signal @30.8% PER	—	—	5	—	dBm
Co-channel C/I	—	—	3	—	dB
Adjacent channel selectivity C/I	F = F0 + 1 MHz	—	–2	—	dB
	F = F0 – 1 MHz	—	–3	—	dB
	F = F0 + 2 MHz	—	–32	—	dB
	F = F0 – 2 MHz	—	–33	—	dB
	F = F0 + 3 MHz	—	–23	—	dB
	F = F0 – 3 MHz	—	–40	—	dB
	F $\geq$ F0 + 4 MHz	—	–34	—	dB
	F $\leq$ F0 – 4 MHz	—	–44	—	dB
Image frequency	—	—	–34	—	dB
Adjacent channel to image frequency	F = F_{image} + 1 MHz	—	–46	—	dB
	F = F_{image} – 1 MHz	—	–23	—	dB

5. Package Information



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	2.6	2.7	2.8
	Y	E2	2.6	2.7	2.8
LEAD LENGTH		L	0.25	0.35	0.45
LEAD TIP TO EXPOSED PAD EDGE		K		0.3 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
		ddd		0.05	
EXPOSED PAD OFFSET		fff		0.1	



NOTES
1.REFER TO JEDEC MO-220;
2.COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD;
3.BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATE SUBSTANCES;
4.FINISH: Cu/EP · Sn8~20s

Figure 9: QFN28 (4×4 mm) Package

Note:

- All dimensions are in millimeters.
- For information about tape, reel, and product marking, please refer to *Espressif Chip Packaging Information*.

6. Related Documentation and Resources

Related Documentation

- *Certificates*
  https://espressif.com/en/support/documents/certificates
- *Documentation Updates and Update Notification Subscription*
  https://espressif.com/en/support/download/documents

Developer Zone

- *ESP-IDF* and other development frameworks on GitHub.
  https://github.com/espressif
- *ESP32 BBS Forum* – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.
  https://esp32.com/
- *The ESP Journal* – Best Practices, Articles, and Notes from Espressif folks.
  https://blog.espressif.com/
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.
  https://espressif.com/en/support/download/sdks-demos

Products

- *ESP8685 Series SoCs* – Browse through all ESP8685 SoCs.
  https://espressif.com/en/products/socs?id=ESP8685
- *ESP8685 Series Modules* – Browse through all ESP8685-based modules.
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Revision History

Date	Version	Release Notes
2022-04-08	v1.0	• Added a new variant ESP8685H4; • Updated Figure *Block Diagram* to show power modes; • Added CoreMark score in Features; • Updated Figure *ESP8685 Power Scheme* and related descriptions; • Updated Table *Peripheral Signals via GPIO Matrix*; • Added note 2 to Table *Recommended Operating Conditions*; • Other updates to wording.
2021-07-30	v0.5	Preliminary release

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