USB PD and other multi-fast charging protocol power receiving chip CH224

Chinese

manual

version: 1F http://wch.cn

1 Overview

CH224 single chip integrates USB PD and other fast charging protocols, supports PD3.0/2.0, BC1.2 and other boost fast charging protocols, automatically detects VCONN and analog E-Mark chip, supports up to 100W power, built-in PD communication module, High integration level, simplified peripheral. Integrated output voltage detection function, and provide over-temperature, over-voltage protection and other functions. It can be widely used in various electronic devices to expand high-power input, such as wireless chargers, electric toothbrushes, rechargeable shavers, lithium battery power tools and other applications.

2. Features

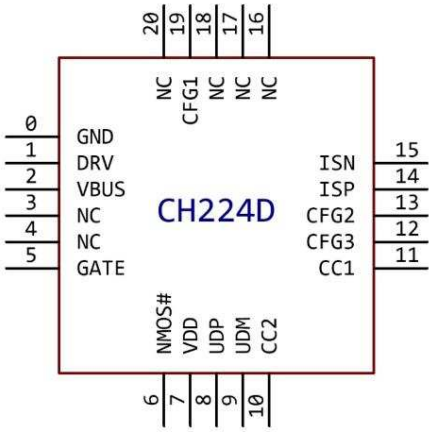
I Support 4V to 22V input voltage I Support PD3.0/2.0, BC1.2 and other fast charging protocols I Support USB Type-C PD, support positive and negative plug detection and automatic switching I Support E-Mark simulation, automatic detection of VCONN, support 100W power PD request I The request voltage can be dynamically adjusted through various methods I High single-chip integration, simplified peripherals, low cost I Built-in overvoltage protection module OVA, over-temperature protection module OTA

3. Applications

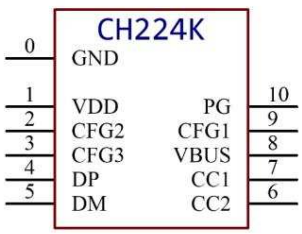
I Wireless Charger I Laptop Charging Cable I Lithium Battery Small Appliances I Lithium Battery Power Tool I Power Bank

4. Pins

4.1. CH224 each package pin arrangement



QFN20-3*3



ESSOP-10

SOT23-6L

4.2. CH221K pin function description

pin number	Pin Name Type		Pin Description
'	VDD		Power working power input, external 1uF decoupling capacitor, series resistance to VBUS working
2	GND		power common ground power supply
3	PG open-drain output default Power Good indicator, active low, customizable functions		
4,5	CC1, CC2 bi-directional		Type-C CC bus power
6	CFG analog input		level configuration input

4.3. CH224K pin function description

pin number	Pin Name Type		Pin Description
0	GND		Common ground terminal of power supply, working power input of power supply for
'	VDD		heat dissipation bottom board, external 1uF decoupling capacitor, series resistor to VBUS
4,5	DP, DM two-way		usb bus
6,7	CC1, CC2 bi-directional		Type-C CC bus
2,3,9	CFG1,CFG2, CFG3	analog input	Power level configuration input
8	VBUS analog input voltage detection input, requires series resistor to external input VBUS		
10	PG open-drain output default Power Good indicator, active low, customizable functions		

4.4. CH224D pin function description

pin number CH224D	Pin Name Type		Pin Description
0	GND	power	Common ground terminal, cooling base
2	VBUS	supply	plate working power input
7	VDD	power supply	internal voltage regulator output terminal, external 1uF decoupling capacitor
8ÿ9	DP, DM two-way		usb bus
10ÿ11 19ÿ	CC1, CC2 bi-directional		Type-C CC bus
13ÿ12	CFG1~3 Input CFG1 is analog input, CFG2, 3 are digital input with built-in pull-down		
'	DRV analog output		Weak drive output, used to drive configuration
14ÿ15	ISP,ISN differential input		resistors for detecting operating current, custom
5	GATE high voltage output		function for driving high-side power path NMOS, custom function
6	NMOS# digital input		GATE pin drives NMOS enable, active low

5. Functional description

5.1. Overview

CH224 is a protocol power receiver IC that supports PD3.0/2.0, BC1.2 and other boost fast charge protocol input, supports voltage requests within the range of 4-22V, and can dynamically configure priority requests in various ways voltage range.

CH221K only supports PD3.0/2.0 protocol.

CH224K/CH224D provides single resistor configuration and level configuration. CH221K only provides single resistor configuration.

5.2. CH224K/CH224D voltage range configuration 5.2.1 Single

resistor configuration is suitable for applications where the same

PCB achieves different requested voltages by modifying the resistance value of the resistor.

CFG1 connects resistors to GND, and different resistance values correspond to different voltage request gears. When using single-resistor configuration, the CFG2 and CFG3 pins Can be suspended. The resistance-request voltage comparison table is as follows.

CFG1 upper resistance	request voltage
6.8Kÿ	9V
24Kÿ	12V
56Kÿ	15V
NC	20V

5.2.2 Level configuration

is suitable for applications where the MCU dynamically adjusts the request voltage, or the PCB circuit fixed request voltage.

CFG1, CFG2, and CFG3 are directly connected to the IO port of the external MCU, or directly connected to the VDD/GND pins of the CH224K/CH224D chip, and use the level to configure the request voltage. The truth table is as follows.

CFG1	CFG2	CFG3	request voltage
1	-	-	5V
0	0	0	9V
0	0	1	12V
0	1	1	15V
0	1	0	20V

When using the level configuration method, attention should be paid to the voltage and default state of the IO port used. For CH224K, the input voltage of CFG2/CFG3 pin cannot be higher than 3.7V; for CH224D, the input voltage of CFG2/CFG3 pin cannot be higher than 5V. If the MCU and other back-end circuits start slowly, or the MCU pins have a specific default state, CFG1 may be in a floating state or IO configuration mode before starting, and 20V may be requested at this time. If the system cannot withstand 20V input, Then a configuration resistor should be added to the CFG1 pin to ensure that before the MCU starts, the CH224K/CH224D can be configured through the resistor to request an appropriate voltage.

5.3. CH221K voltage range configuration

CFG connects resistance to VDD, and different resistance values correspond to different voltage request gears. The resistance-request voltage comparison table

CFG to VDD resistance	is as follows. request voltage
10Kÿ	5V
20Kÿ	9V
47Kÿ	12V
100Kÿ	15V
200Kÿ	20V

5.4. Simulate E-Mark function

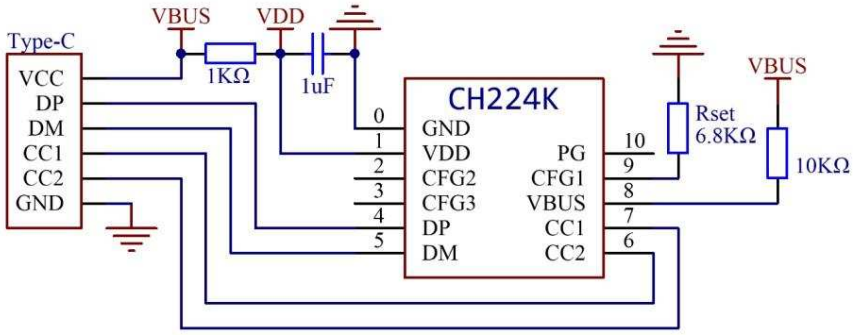
If you want to use the analog E-Mark function to request an output greater than 20V or greater than 60W, you must use a Type-C male connector and connect it to the CC2 Connect a 1Kÿ resistor to GND. (Please consult our technical support)

5.5. Use PD protocol only

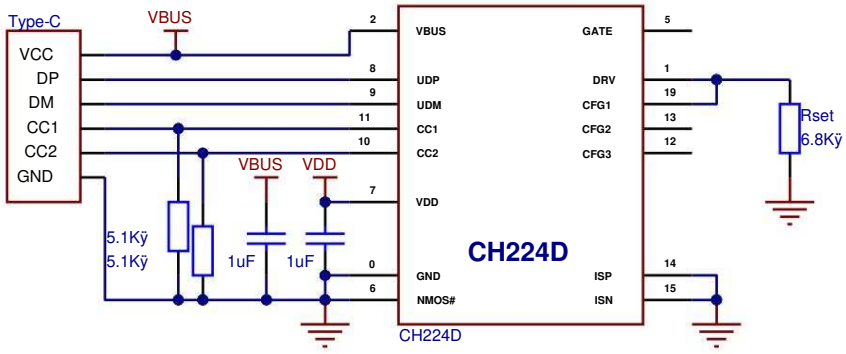
If you don't need to use A port protocol (various protocols realized by DP, DM communication), you can choose CH221K model. If you want to shield these protocols on CH224K/CH224D, you need to disconnect the DP/DM pin of CH224K/CH224D from the Type-C interface. DP/DM connection, and short-circuit DP and DM on CH224K/CH224D side. For CH224K, the VBUS pin can be NC at this time.

6. Reference Schematic

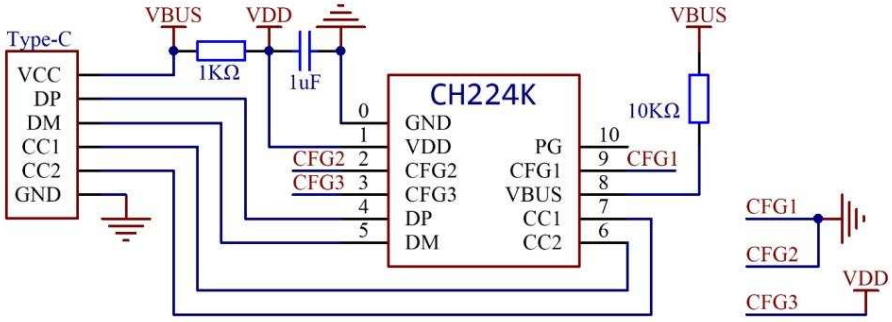
6.1. CH224K/CH224D use Type-C female port, single resistor configuration 9/12/15/20V (resistor configuration 6.8Kÿ in the figure is 9v)



Rset resistance request voltage	
6.8Kÿ	9V
24Kÿ	12V
56Kÿ	15V
NC	20V

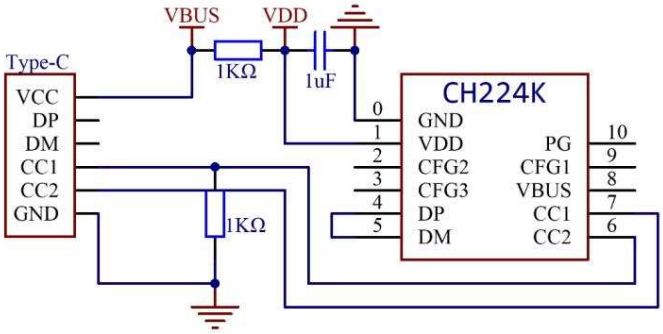


6.2. CH224K uses Type-C female port, the level configuration is 5/9/12/15/20V (the level configuration in the figure is 12v)

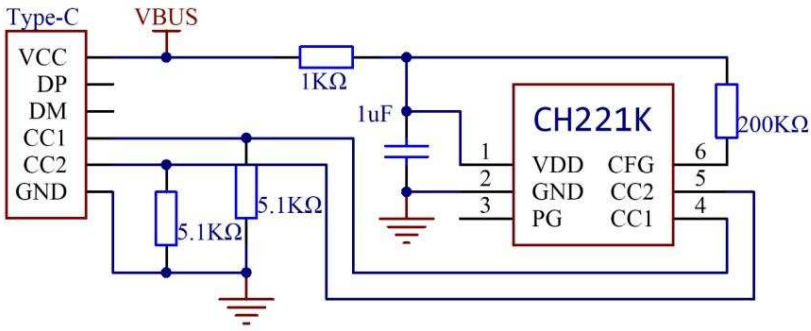


CFG1	CFG2	CFG3	request voltage
,	,	,	5V
0	0	0	9V
0	0	,	12V
0	,	,	15V
0	,	0	20V

6.3. CH224K uses Type-C male port, only uses PD protocol and E-Mark simulation function (the resistor configuration NC in the figure is 20v)



6.4. CH221K uses Type-C female port, the level configuration is 20V



7. Parameters

7.1. Absolute maximum value of CH221K chip

(Critical or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged)

name	Parameter Description	min	max	unit
PER	Ambient temperature during	-40	105 ÿ	
TS	operation Ambient temperature	-55	150 ÿ	
VDD	during storage Operating power supply voltage (VDD pin connected to power	-0.5	5.8	IN
VODHV	supply, GND pin grounded) Voltage on high-voltage open-drain output pin PG	-0.5	13.5	IN
VIOCC	Voltage on pins CC1, CC2	-0.5	8	IN
VIOUX	The voltage on the CFG pin	-0.5	VDD+0.5	IN
PD	The maximum power consumption of the entire chip (VDD voltage * current)		250	mW

7.2. Absolute maximum value of CH224K chip

(Critical or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged)

name	Parameter Description	min	max	unit
PER	Ambient temperature during	-40	90	ÿ
TS	operation Ambient temperature during storage	-55	105 ÿ	
VDD	Working power supply voltage (VDD pin connected to power supply, GND pin	3.0	3.6	IN
VIOHV	connected to ground) Voltage on pins supporting high voltage (CFG, VBUS)	-0.5	13.5	IN
VIOCC	Voltage on pins CC1, CC2, CFG1	-0.5	8	IN
VIOUX	Voltage on pins DP,DM,CFG,CFG2,CFG3	-0.5	VDD+0.5	IN
VIOLV	Voltage on pin CFGHV		0.8	IN
PD	The maximum power consumption of the whole chip (VDD voltage * current)		400	mW

7.3. The absolute maximum value of the CH224D chip

(critical or exceeding the absolute maximum value may cause the chip to work abnormally or even be damaged)

name	Parameter Description	min max unit		
PER	Ambient temperature at work	-40	100 ÿ	
TS	Ambient temperature during storage	-55	125 ÿ	
VDD	Working power supply voltage (VDD pin connected to power supply, GND pin connected to ground)	-0.5	6	IN
VIOHV	Voltage on VBUS pin	-0.5	24	IN
VIOCC	Voltage on pins CC1, CC2	-0.5	20	IN
VIOUX	Voltage on DP,DM,CFG1,CFG2,CFG3,DRV,NMOS#,ISP,ISN pins-0.5 VDD+0.5			IN
VIOHX	Voltage on GATE pin	-0.5VIOHV+6.5V		
PD	The maximum power consumption of the whole chip (VDD voltage * current)		300	mW

7.4. Electrical parameters of CH221K chip (test condition: TA=25ÿ)

name	Parameter Description	Min Typ Max Unit			
VLDOK	CH221K internal power regulator VDD parallel voltage regulator	3.0	3.3	3.6	IN
IN LINE	Internal Power Regulator VDD Parallel Sink Current Capability	0		30	mA
VR	Voltage threshold for power-on reset	2.2	2.4	2.6	IN

7.5. Electrical parameters of CH224K chip (test condition: TA=25ÿ)

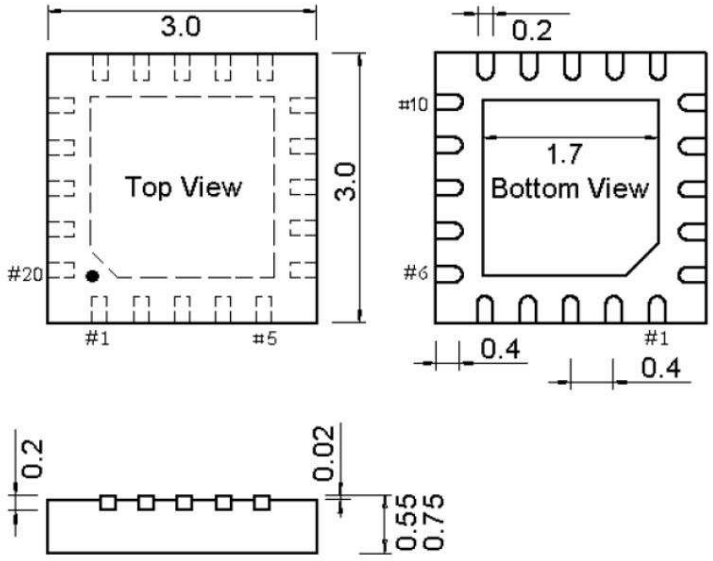
name	Parameter Description	Min Typ Max Unit			
VLDOK	CH224K Internal power regulator VDD Parallel voltage	3.24	3.3	3.36	IN
IN LINE	regulator Internal power regulator VDD Parallel sink current	0		30	mA
ALL	capability Over-temperature protection module OTA	90	105	120 ÿ	
VR	reference threshold temperature Voltage threshold of power-on reset	2.2	2.4	2.6	IN

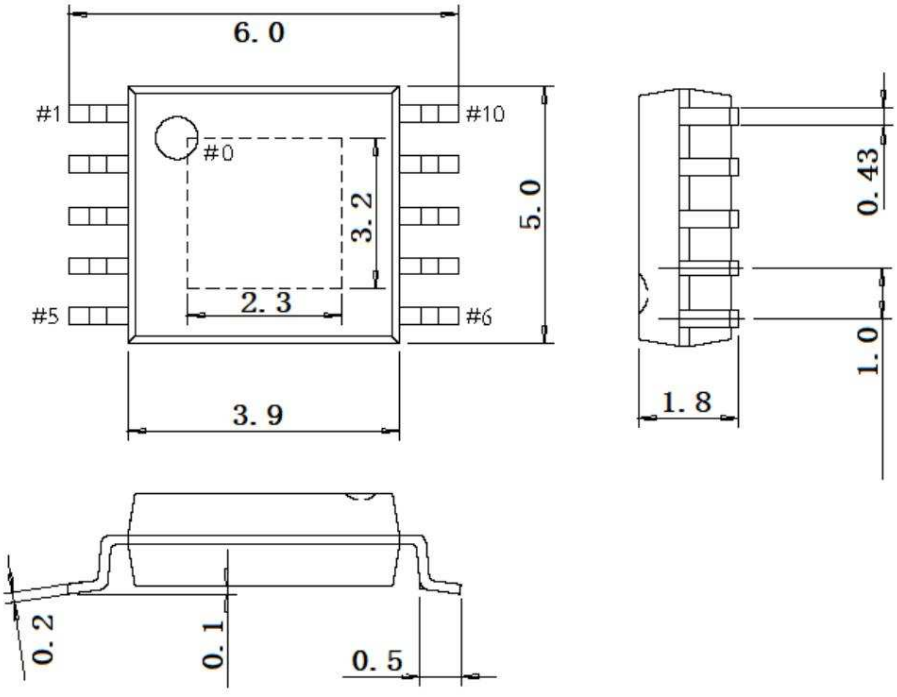
7.6. Electrical parameters of CH224D chip (test condition: TA=25ÿ)

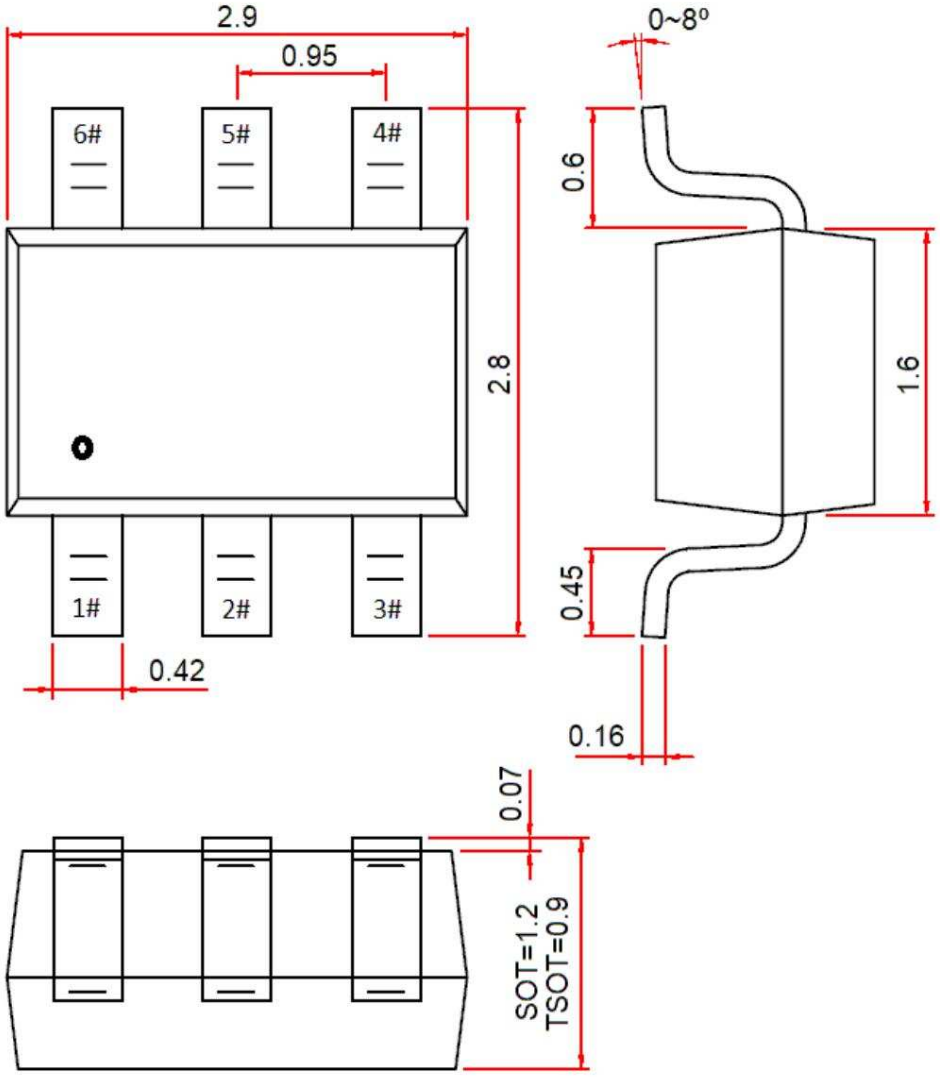
name	Parameter Description	Min Typ Max Unit			
VLDO	Internal power regulator VDD output voltage	4.65	4.7	4.75	IN
IN LINE	Internal power regulator VDD External load capacity			10	mA
VR	Power-on reset voltage threshold	2.2	2.4	2.6	IN

8. Packaging Information

Package form	Plastic body width		Pin spacing		Package	ordering model
QFN20	3*3mm	118mil	Description 0.40mm 15.7mil Quad Flat No Lead Package CH224D 39mil Narrow Pitch 10-Pin			
ESSOP10	3.9mm	150mil	1.00mm	SMD with Backplane CH224K Small 6-Pin SMD		
SOT23-6L	1.6mm	63 miles	0.95mm	37 miles		CH221K







Note: The unit marked in the package information diagram is mm (millimeter).