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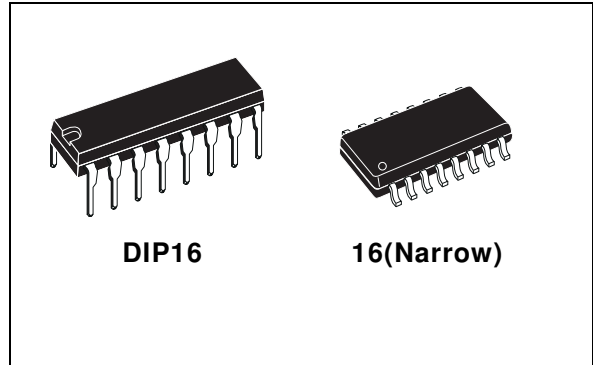
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REGULATING PULSE WIDTH MODULATORS

- 8 TO 35 V OPERATION
- 5.1 V REFERENCE TRIMMED TO $\pm 1\%$
- 100 Hz TO 500 KHz OSCILLATOR RANGE
- SEPARATE OSCILLATOR SYNC TERMINAL
- ADJUSTABLE DEADTIME CONTROL
- INTERNAL SOFT-START
- PULSE-BY-PULSE SHUTDOWN
- INPUT UNDERVOLTAGE LOCKOUT WITH HYSTERESIS
- LATCHING PWM TO PREVENT MULTIPLE PULSES
- DUAL SOURCE/SINK OUTPUT DRIVERS

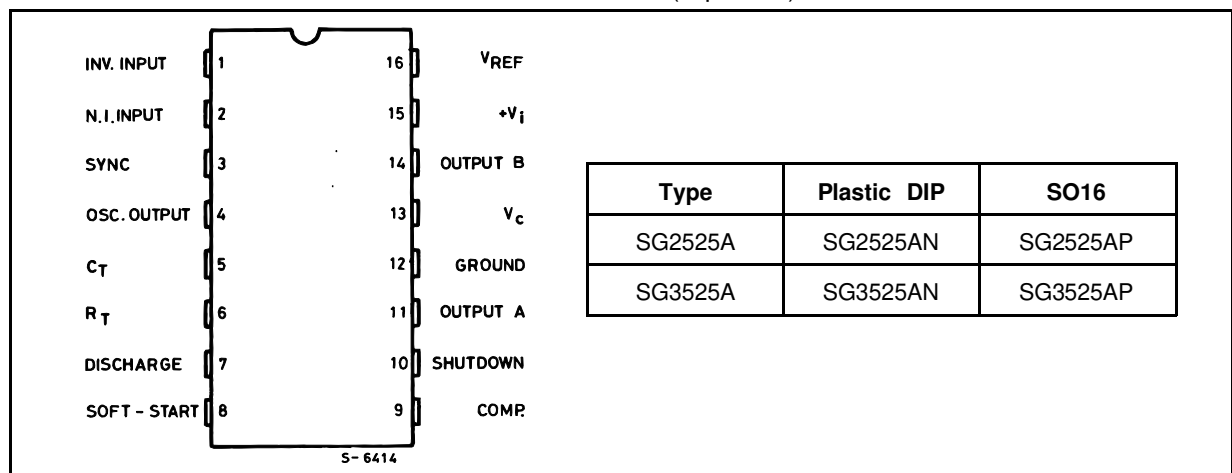


DESCRIPTION

The SG3525A series of pulse width modulator integrated circuits are designed to offer improved performance and lowered external parts count when used in designing all types of switching power supplies. The on-chip + 5.1 V reference is trimmed to $\pm 1\%$ and the input common-mode range of the error amplifier includes the reference voltage eliminating external resistors. A sync input to the oscillator allows multiple units to be slaved or a single unit to be synchronized to an external system clock. A single resistor between the C_T and the discharge terminals provide a wide range of dead time adjustment. These devices also feature built-in soft-start circuitry with only an external timing capacitor required. A shutdown terminal controls both the soft-start circuitry and the output stages, providing instantaneous

turn off through the PWM latch with pulsed shutdown, as well as soft-start recycle with longer shutdown commands. These functions are also controlled by an undervoltage lockout which keeps the outputs off and the soft-start capacitor discharged for sub-normal input voltages. This lockout circuitry includes approximately 500 mV of hysteresis for jitter-free operation. Another feature of these PWM circuits is a latch following the comparator. Once a PWM pulse has been terminated for any reason, the outputs will remain off for the duration of the period. The latch is reset with each clock pulse. The output stages are totem-pole designs capable of sourcing or sinking in excess of 200 mA. The SG3525A output stage features NOR logic, giving a LOW output for an OFF state.

PIN CONNECTIONS AND ORDERING NUMBERS (top view)



SG2525A-SG3525A

ABSOLUTE MAXIMUM RATINGS

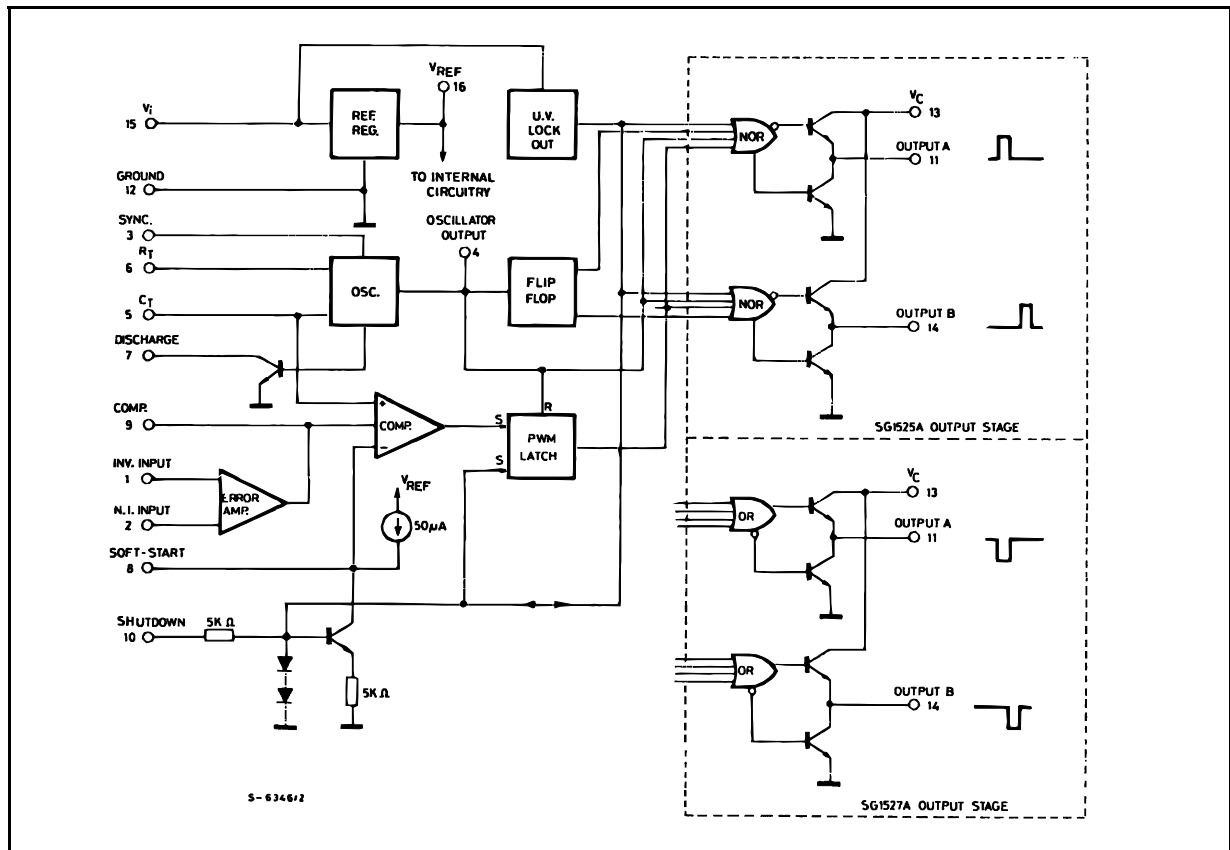
| Symbol | Parameter | Value | Unit |
|-----------|--|-----------------------|--------------------------------------|
| V_i | Supply Voltage | 40 | V |
| V_C | Collector Supply Voltage | 40 | V |
| I_{OSC} | Oscillator Charging Current | 5 | mA |
| I_o | Output Current, Source or Sink | 500 | mA |
| I_R | Reference Output Current | 50 | mA |
| I_T | Current through C_T Terminal | 5 | mA |
| | Logic Inputs | - 0.3 to + 5.5 | V |
| | Analog Inputs | - 0.3 to V_i | V |
| P_{tot} | Total Power Dissipation at $T_{amb} = 70^\circ\text{C}$ | 1000 | mW |
| T_j | Junction Temperature Range | - 55 to 150 | $^\circ\text{C}$ |
| T_{stg} | Storage Temperature Range | - 65 to 150 | $^\circ\text{C}$ |
| T_{op} | Operating Ambient Temperature : SG2525A SG3525A | - 25 to 85 0 to 70 | $^\circ\text{C}$ $^\circ\text{C}$ |

THERMAL DATA

| Symbol | Parameter | | SO16 | DIP16 | Unit |
|---------------------|---|-----|------|-------|---------------------------|
| $R_{th\ j-pins}$ | Thermal Resistance Junction-pins | Max | | 50 | $^\circ\text{C}/\text{W}$ |
| $R_{th\ j-amb}$ | Thermal Resistance Junction-ambient | Max | | 80 | $^\circ\text{C}/\text{W}$ |
| $R_{th\ j-alumina}$ | Thermal Resistance Junction-alumina (*) | Max | 50 | | $^\circ\text{C}/\text{W}$ |

* Thermal resistance junction-alumina with the device soldered on the middle of an alumina supporting substrate measuring 15×20 mm ; 0.65 mm thickness with infinite heatsink.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

($V_i = 20\text{ V}$, and over operating temperature, unless otherwise specified)

| Symbol | Parameter | Test Conditions | SG2525A | | | SG3525A | | | Unit |
|---|--------------------------|--|---------|-----------|---------|---------|---------|---------|------------------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| REFERENCE SECTION | | | | | | | | | |
| V_{REF} | Output Voltage | $T_j = 25\text{ }^\circ\text{C}$ | 5.05 | 5.1 | 5.15 | 5 | 5.1 | 5.2 | V |
| ΔV_{REF} | Line Regulation | $V_i = 8\text{ to }35\text{ V}$ | | 10 | 20 | | 10 | 20 | mV |
| ΔV_{REF} | Load Regulation | $I_L = 0\text{ to }20\text{ mA}$ | | 20 | 50 | | 20 | 50 | mV |
| $\Delta V_{REF}/\Delta T^*$ | Temp. Stability | Over Operating Range | | 20 | 50 | | 20 | 50 | mV |
| * | Total Output Variation | Line, Load and Temperature | 5 | | 5.2 | 4.95 | | 5.25 | V |
| | Short Circuit Current | $V_{REF} = 0\text{ } T_j = 25\text{ }^\circ\text{C}$ | | 80 | 100 | | 80 | 100 | mA |
| * | Output Noise Voltage | 10 Hz $\leq f \leq$ 10 kHz, $T_j = 25\text{ }^\circ\text{C}$ | | 40 | 200 | | 40 | 200 | μVrms |
| ΔV_{REF}^* | Long Term Stability | $T_j = 125\text{ }^\circ\text{C}$, 1000 hrs | | 20 | 50 | | 20 | 50 | mV |
| OSCILLATOR SECTION ** | | | | | | | | | |
| *, • | Initial Accuracy | $T_j = 25\text{ }^\circ\text{C}$ | | ± 2 | ± 6 | | ± 2 | ± 6 | % |
| *, • | Voltage Stability | $V_i = 8\text{ to }35\text{ V}$ | | ± 0.3 | ± 1 | | ± 1 | ± 2 | % |
| $\Delta f/\Delta T^*$ | Temperature Stability | Over Operating Range | | ± 3 | ± 6 | | ± 3 | ± 6 | % |
| f_{MIN} | Minimum Frequency | $R_T = 200\text{ K}\Omega\text{ } C_T = 0.1\text{ }\mu\text{F}$ | | | 120 | | | 120 | Hz |
| f_{MAX} | Maximum Frequency | $R_T = 2\text{ K}\Omega\text{ } C_T = 470\text{ pF}$ | 400 | | | 400 | | | KHz |
| | Current Mirror | $I_{RT} = 2\text{ mA}$ | 1.7 | 2 | 2.2 | 1.7 | 2 | 2.2 | mA |
| *, • | Clock Amplitude | | 3 | 3.5 | | 3 | 3.5 | | V |
| *, • | Clock Width | $T_j = 25\text{ }^\circ\text{C}$ | 0.3 | 0.5 | 1 | 0.3 | 0.5 | 1 | μs |
| | Sync Threshold | | 1.2 | 2 | 2.8 | 1.2 | 2 | 2.8 | V |
| | Sync Input Current | Sync Voltage = 3.5 V | | 1 | 2.5 | | 1 | 2.5 | mA |
| ERROR AMPLIFIER SECTION ($V_{CM} = 5.1\text{ V}$) | | | | | | | | | |
| V_{OS} | Input Offset Voltage | | | 0.5 | 5 | | 2 | 10 | mV |
| I_b | Input Bias Current | | | 1 | 10 | | 1 | 10 | μA |
| I_{os} | Input Offset Current | | | | 1 | | | 1 | μA |
| | DC Open Loop Gain | $R_L \geq 10\text{ M}\Omega$ | 60 | 75 | | 60 | 75 | | dB |
| * | Gain Bandwidth Product | $G_v = 0\text{ dB } T_j = 25\text{ }^\circ\text{C}$ | 1 | 2 | | 1 | 2 | | MHz |
| *, ■ | DC Transconduct. | $30\text{ K}\Omega \leq R_L \leq 1\text{ M}\Omega$ $T_j = 25\text{ }^\circ\text{C}$ | 1.1 | 1.5 | | 1.1 | 1.5 | | ms |
| | Output Low Level | | | 0.2 | 0.5 | | 0.2 | 0.5 | V |
| | Output High Level | | 3.8 | 5.6 | | 3.8 | 5.6 | | V |
| CMR | Comm. Mode Reject. | $V_{CM} = 1.5\text{ to }5.2\text{ V}$ | 60 | 75 | | 60 | 75 | | dB |
| PSR | Supply Voltage Rejection | $V_i = 8\text{ to }35\text{ V}$ | 50 | 60 | | 50 | 60 | | dB |

SG2525A-SG3525A

ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Conditions | SG2525A | | | SG3525A | | | Unit |
|--|------------------------|---|---------|------|------|---------|------|------|------|
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| PWM COMPARATOR | | | | | | | | | |
| | Minimum Duty-cycle | | | | 0 | | | 0 | % |
| • | Maximum Duty-cycle | | 45 | 49 | | 45 | 49 | | % |
| • | Input Threshold | Zero Duty-cycle | 0.7 | 0.9 | | 0.7 | 0.9 | | V |
| | | Maximum Duty-cycle | | 3.3 | 3.6 | | 3.3 | 3.6 | V |
| * | Input Bias Current | | | 0.05 | 1 | | 0.05 | 1 | μA |
| SHUTDOWN SECTION | | | | | | | | | |
| | Soft Start Current | $V_{SD} = 0\text{ V}, V_{SS} = 0\text{ V}$ | 25 | 50 | 80 | 25 | 50 | 80 | μA |
| | Soft Start Low Level | $V_{SD} = 2.5\text{ V}$ | | 0.4 | 0.7 | | 0.4 | 0.7 | V |
| | Shutdown Threshold | To outputs, $V_{SS} = 5.1\text{ V}$ $T_j = 25\text{ °C}$ | 0.6 | 0.8 | 1 | 0.6 | 0.8 | 1 | V |
| | Shutdown Input Current | $V_{SD} = 2.5\text{ V}$ | | 0.4 | 1 | | 0.4 | 1 | mA |
| * | Shutdown Delay | $V_{SD} = 2.5\text{ V } T_j = 25\text{ °C}$ | | 0.2 | 0.5 | | 0.2 | 0.5 | μs |
| OUTPUT DRIVERS (each output) ($V_C = 20\text{ V}$) | | | | | | | | | |
| | Output Low Level | $I_{\text{sink}} = 20\text{ mA}$ | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| | | $I_{\text{sink}} = 100\text{ mA}$ | | 1 | 2 | | 1 | 2 | V |
| | Output High Level | $I_{\text{source}} = 20\text{ mA}$ | 18 | 19 | | 18 | 19 | | V |
| | | $I_{\text{source}} = 100\text{ mA}$ | 17 | 18 | | 17 | 18 | | V |
| | Under-Voltage Lockout | V_{comp} and $V_{\text{ss}} = \text{High}$ | 6 | 7 | 8 | 6 | 7 | 8 | V |
| I_C | Collector Leakage | $V_C = 35\text{ V}$ | | | 200 | | | 200 | μA |
| t_r^* | Rise Time | $C_L = 1\text{ nF}, T_j = 25\text{ °C}$ | | 100 | 600 | | 100 | 600 | ns |
| t_f^* | Fall Time | $C_L = 1\text{ nF}, T_j = 25\text{ °C}$ | | 50 | 300 | | 50 | 300 | ns |
| TOTAL STANDBY CURRENT | | | | | | | | | |
| I_s | Supply Current | $V_i = 35\text{ V}$ | | 14 | 20 | | 14 | 20 | mA |

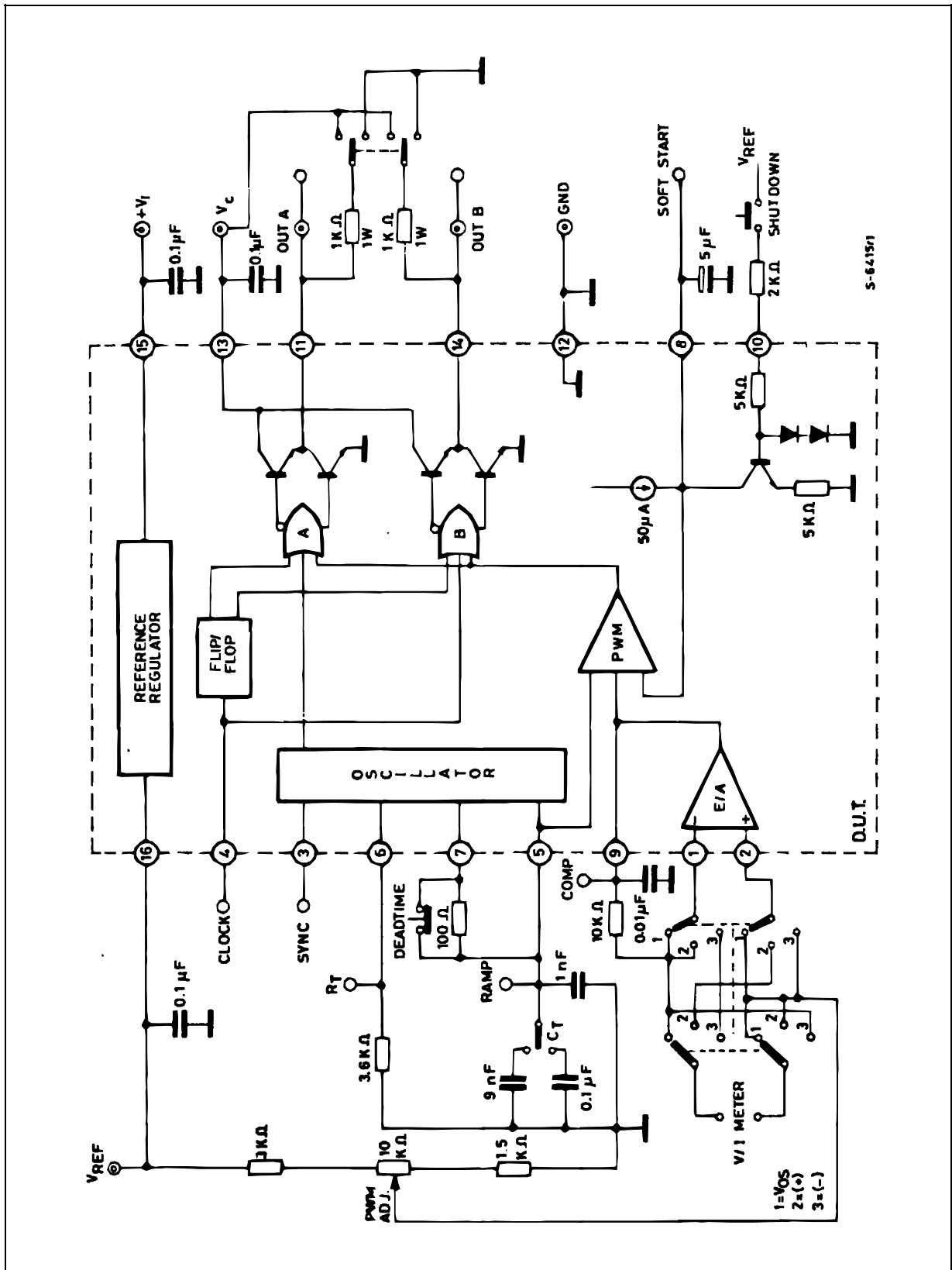
* These parameters, although guaranteed over the recommended operating conditions, are not 100 % tested in production.

• Tested at $f_{\text{osc}} = 40\text{ KHz}$ ($R_T = 3.6\text{ K}\Omega$, $C_T = 10\text{ nF}$, $R_D = 0\text{ }\Omega$). Approximate oscillator frequency is defined by :

$$f = \frac{1}{C_T(0.7 R_T + 3 R_D)}$$

■ DC transconductance (g_M) relates to DC open-loop voltage gain (G_v) according to the following equation : $G_v = g_M R_L$ where R_L is the resistance from pin 9 to ground. The minimum g_M specification is used to calculate minimum G_v when the error amplifier output is loaded.

TEST CIRCUIT



RECOMMENDED OPERATING CONDITIONS (•)

| Parameter | Value |
|---|--------------------------------|
| Input Voltage (V_i) | 8 to 35 V |
| Collector Supply Voltage (V_C) | 4.5 to 35 V |
| Sink/Source Load Current (steady state) | 0 to 100 mA |
| Sink/Source Load Current (peak) | 0 to 400 mA |
| Reference Load Current | 0 to 20 mA |
| Oscillator Frequency Range | 100 Hz to 400 KHz |
| Oscillator Timing Resistor | 2 K Ω to 150 K Ω |
| Oscillator Timing Capacitor | 0.001 μ F to 0.1 μ F |
| Dead Time Resistor Range | 0 to 500 Ω |

(•) Range over which the device is functional and parameter limits are guaranteed.

Figure 1 : Oscillator Charge Time vs. R_T and C_T .

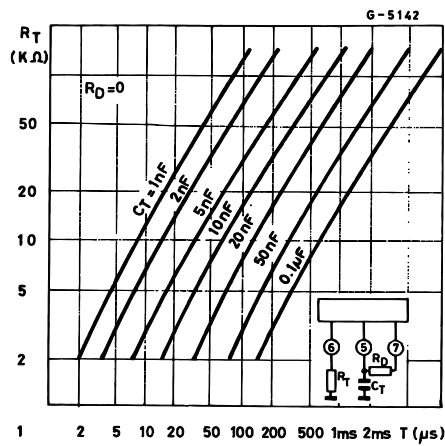


Figure 2 : Oscillator Discharge Time vs. R_D and C_T .

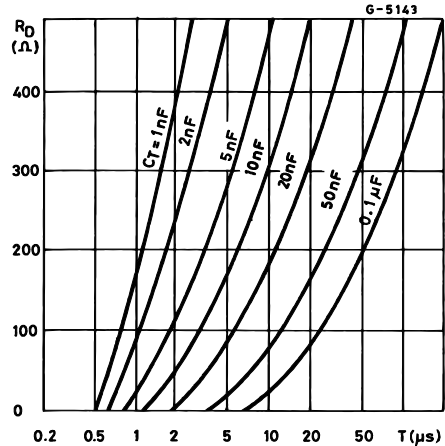


Figure 3 : Output Saturation Characteristics.

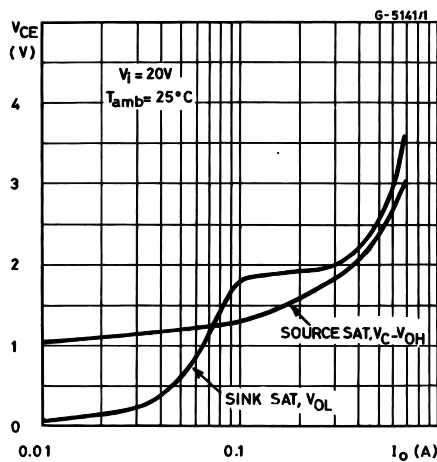


Figure 4 : Error Amplifier Voltage Gain and Phase vs. Frequency.

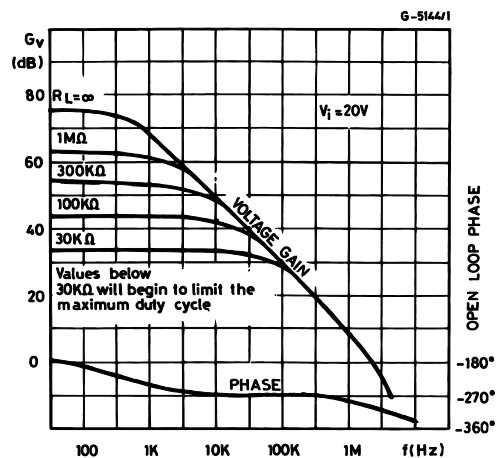
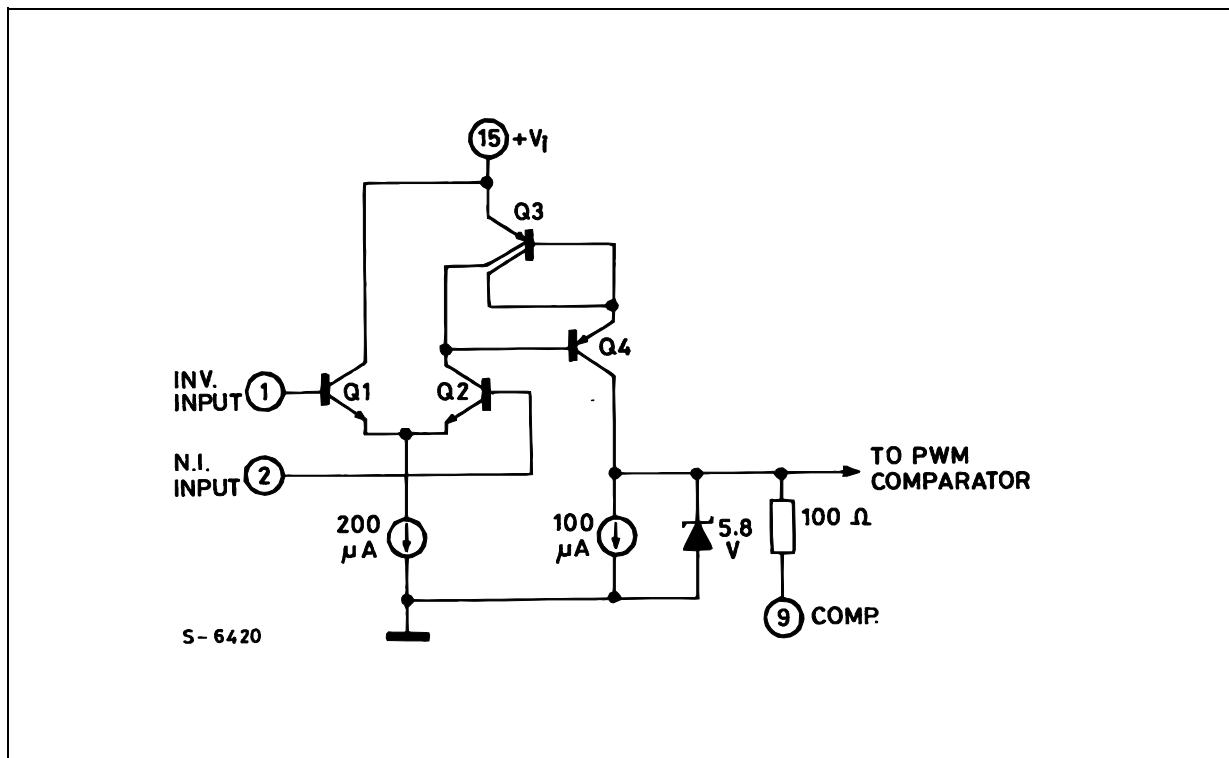


Figure 5 : Error Amplifier.



PRINCIPLES OF OPERATION

SHUTDOWN OPTIONS (see Block Diagram)

Since both the compensation and soft-start terminals (Pins 9 and 8) have current source pull-ups, either can readily accept a pull-down signal which only has to sink a maximum of 100 μA to turn off the outputs. This is subject to the added requirement of discharging whatever external capacitance may be attached to these pins.

An alternate approach is the use of the shutdown circuitry of Pin 10 which has been improved to enhance the available shutdown options. Activating this circuit by applying a positive signal on Pin 10 performs two functions : the PWM latch is immedi-

ately set providing the fastest turn-off signal to the outputs ; and a 150 μA current sink begins to discharge the external soft-start capacitor. If the shutdown command is short, the PWM signal is terminated without significant discharge of the soft-start capacitor, thus, allowing, for example, a convenient implementation of pulse-by-pulse current limiting. Holding Pin 10 high for a longer duration, however, will ultimately discharge this external capacitor, recycling slow turn-on upon release.

Pin 10 should not be left floating as noise pickup could conceivably interrupt normal operation.

Figure 6 : Oscillator Schematic.

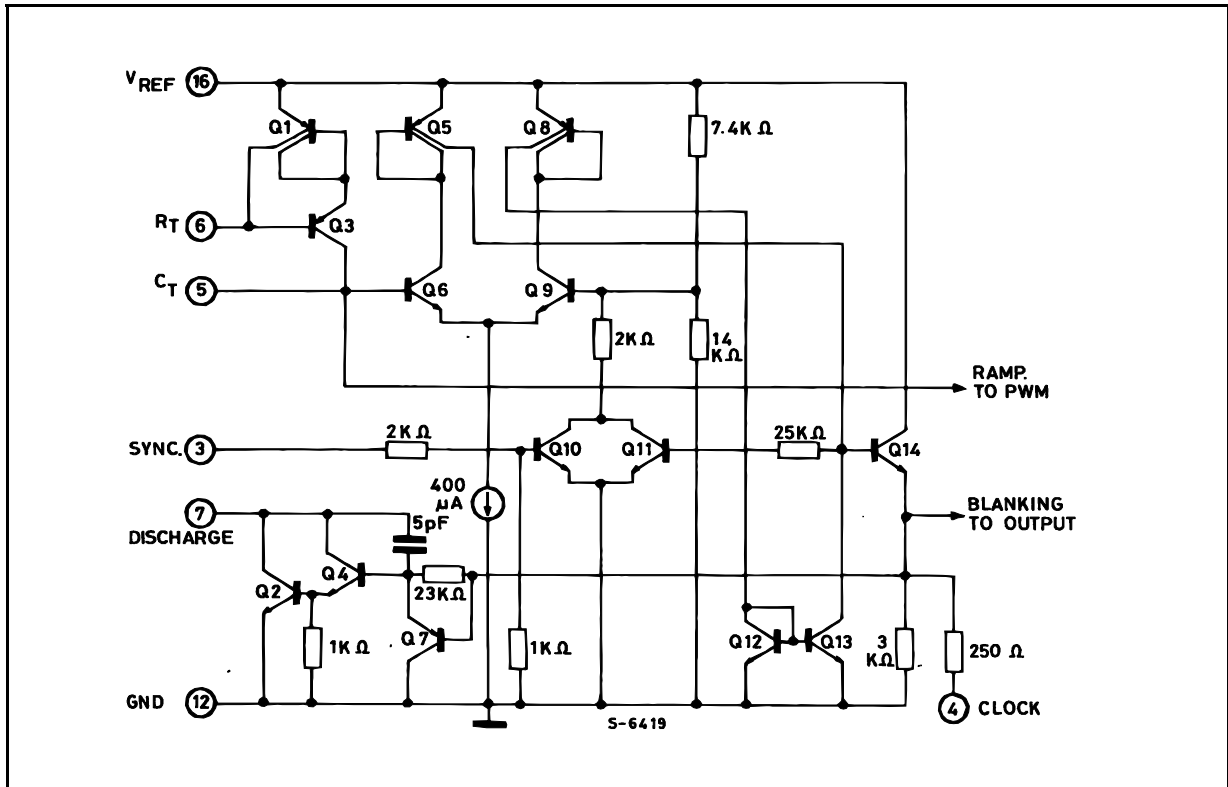


Figure 7 : Output Circuit (1/2 circuit shown).

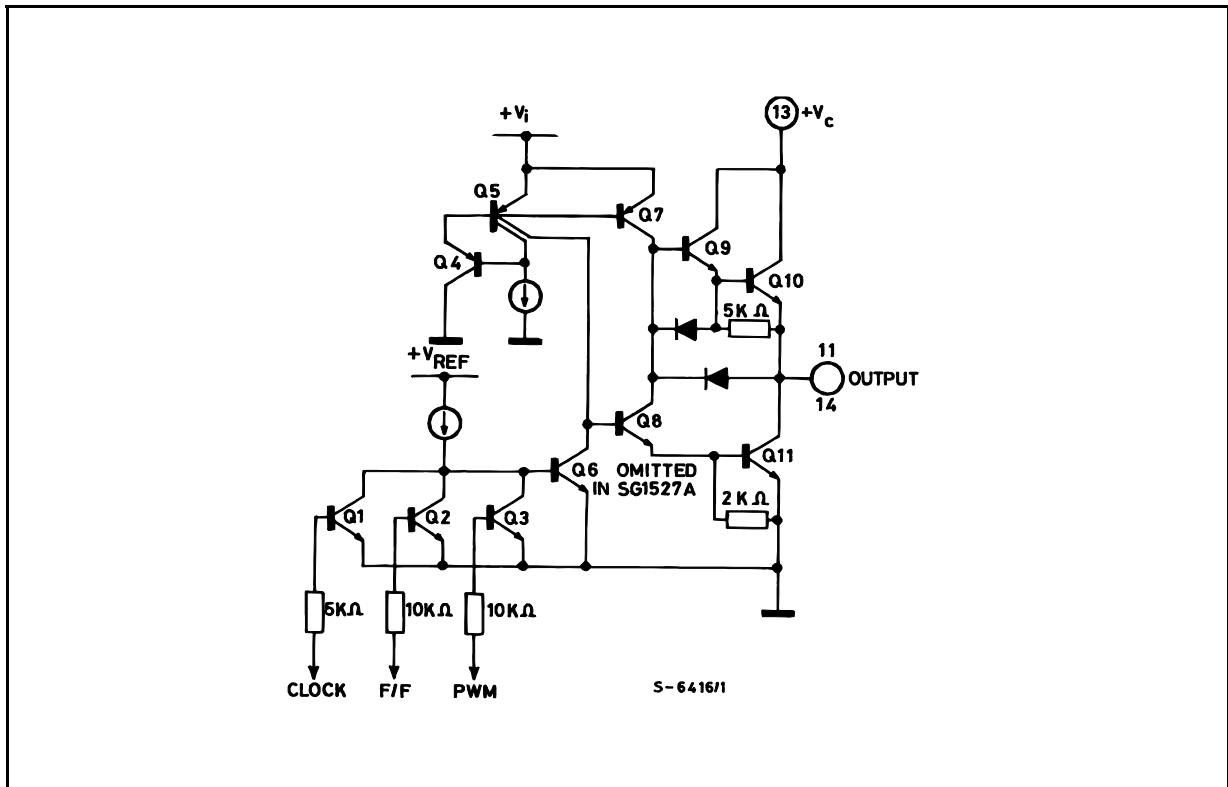
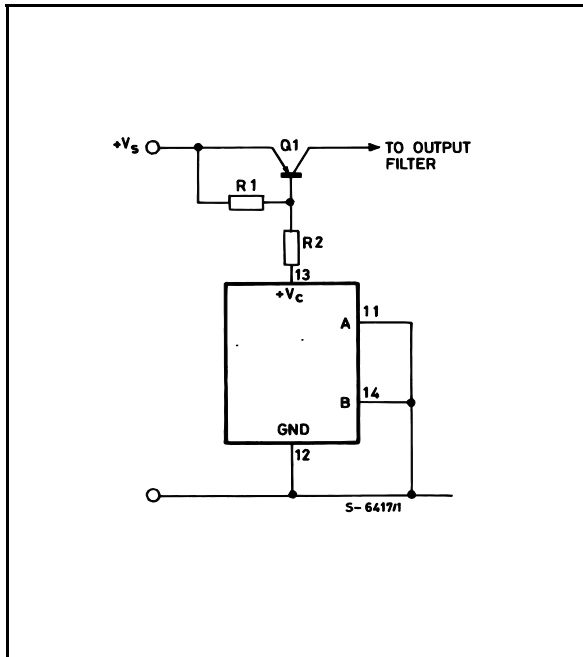
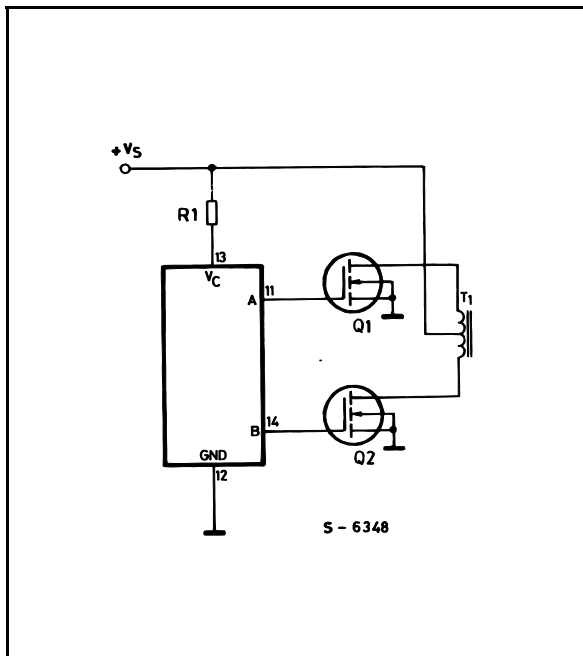


Figure 8.



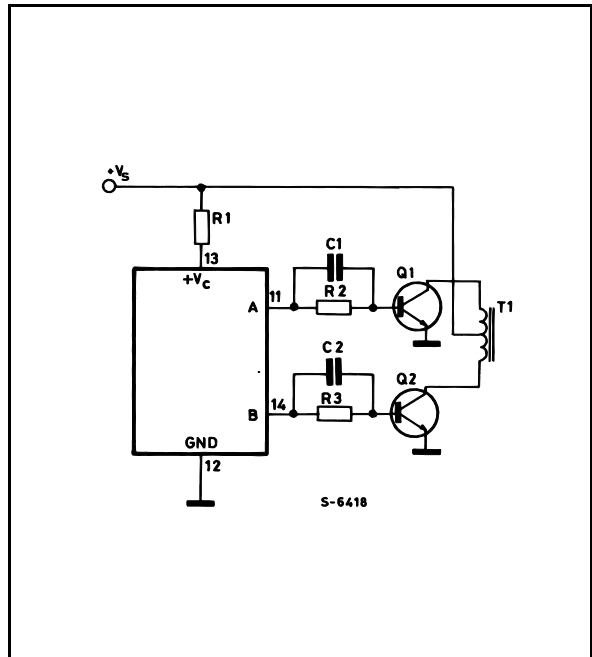
For single-ended supplies, the driver outputs are grounded. The V_c terminal is switched to ground by the totem-pole source transistors on alternate oscillator cycles.

Figure 10.



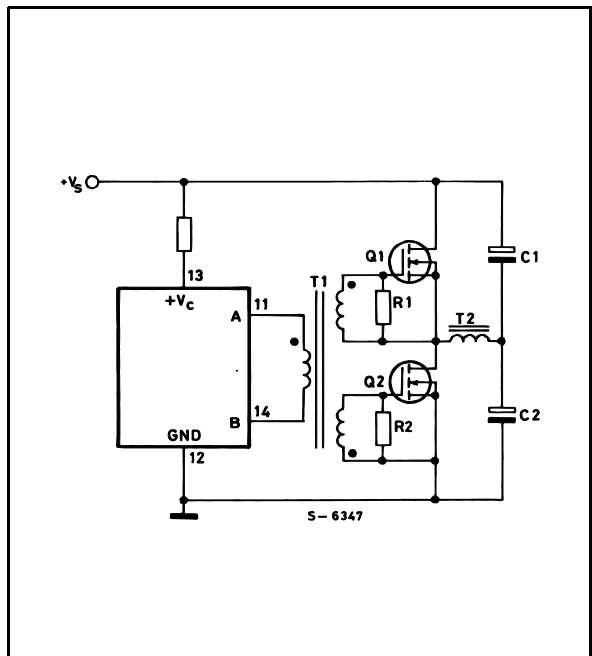
The low source impedance of the output drivers provides rapid charging of Power Mos input capacitance while minimizing external components.

Figure 9.



In conventional push-pull bipolar designs, forward base drive is controlled by $R_1 - R_3$. Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2 .

Figure 11.

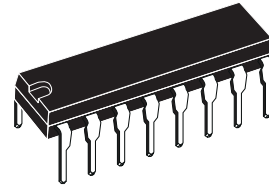


Low power transformers can be driven directly. Automatic reset occurs during dead time, when both ends of the primary winding are switched to ground.

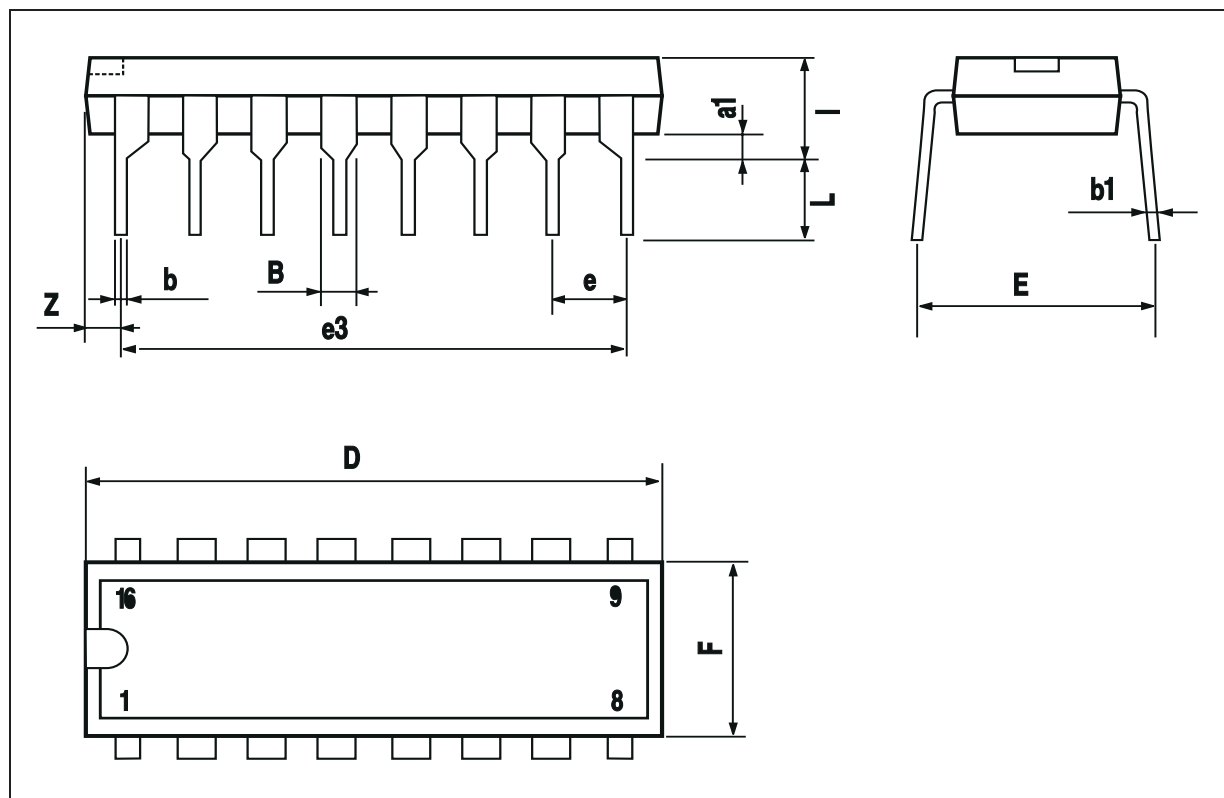
SG2525A-SG3525A

| DIM. | mm | | | inch | | |
|------|------|-------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| a1 | 0.51 | | | 0.020 | | |
| B | 0.77 | | 1.65 | 0.030 | | 0.065 |
| b | | 0.5 | | | 0.020 | |
| b1 | | 0.25 | | | 0.010 | |
| D | | | 20 | | | 0.787 |
| E | | 8.5 | | | 0.335 | |
| e | | 2.54 | | | 0.100 | |
| e3 | | 17.78 | | | 0.700 | |
| F | | | 7.1 | | | 0.280 |
| I | | | 5.1 | | | 0.201 |
| L | | 3.3 | | | 0.130 | |
| Z | | | 1.27 | | | 0.050 |

OUTLINE AND MECHANICAL DATA

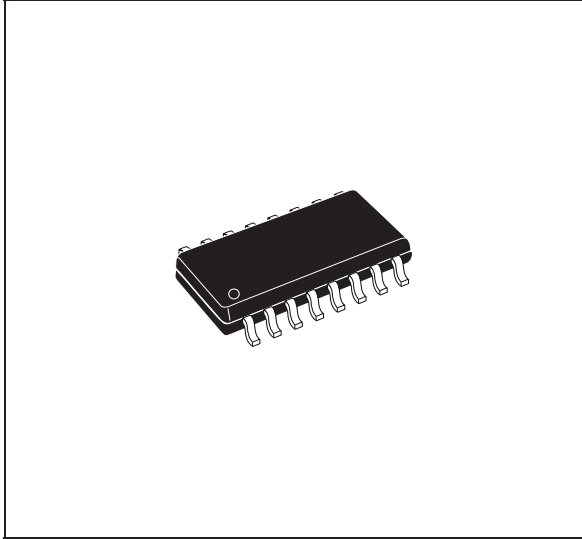


DIP16



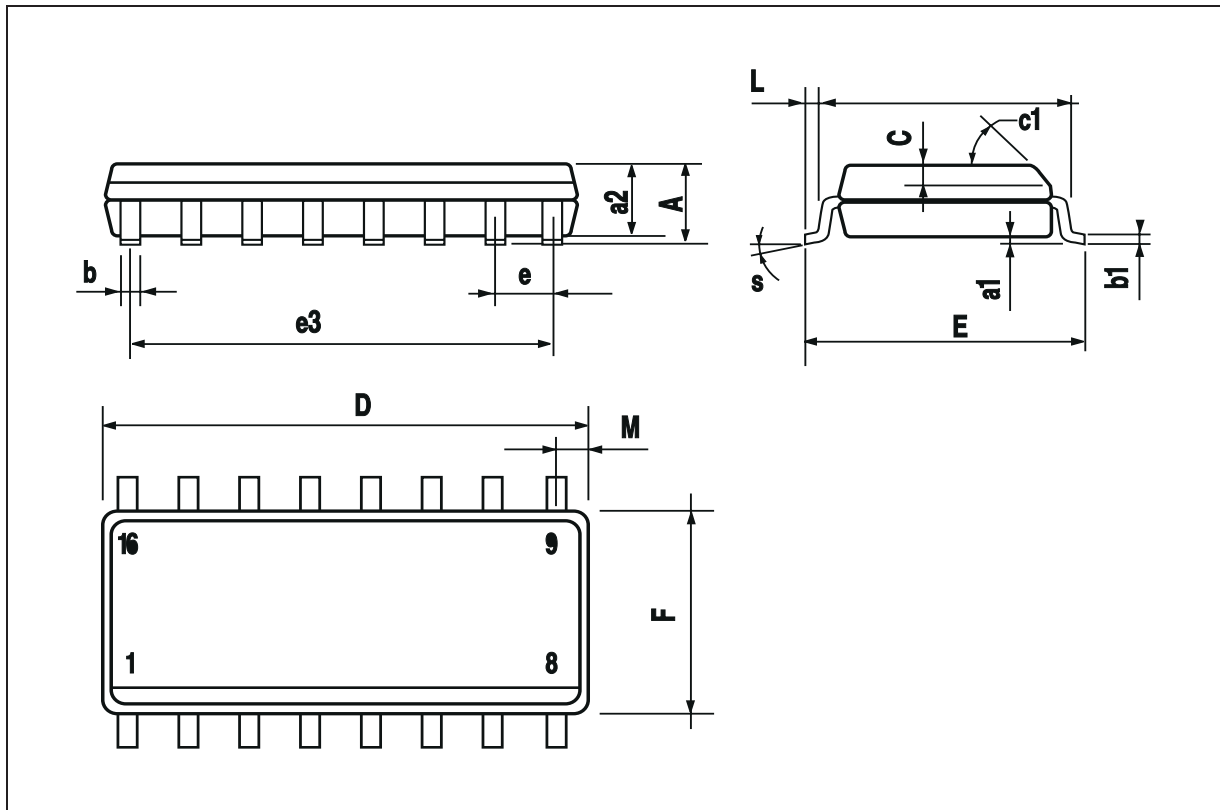
| DIM. | mm | | | inch | | |
|-------|------------|------|------|-------|-------|-------|
| | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. |
| A | | | 1.75 | | | 0.069 |
| a1 | 0.1 | | 0.25 | 0.004 | | 0.009 |
| a2 | | | 1.6 | | | 0.063 |
| b | 0.35 | | 0.46 | 0.014 | | 0.018 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.5 | | | 0.020 | |
| c1 | 45° (typ.) | | | | | |
| D (1) | 9.8 | | 10 | 0.386 | | 0.394 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 8.89 | | | 0.350 | |
| F (1) | 3.8 | | 4 | 0.150 | | 0.157 |
| G | 4.6 | | 5.3 | 0.181 | | 0.209 |
| L | 0.4 | | 1.27 | 0.016 | | 0.050 |
| M | | | 0.62 | | | 0.024 |
| S | 8°(max.) | | | | | |

OUTLINE AND MECHANICAL DATA



SO16 Narrow

(1) D and F do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (.006inch).



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