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DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT153 Dual 4-input multiplexer

Product specification
File under Integrated Circuits, IC06

December 1990

Dual 4-input multiplexer

74HC/HCT153

FEATURES

- Non-inverting output
- Separate enable for each output
- Common select inputs
- See ‘253’ for 3-state version
- Permits multiplexing from n lines to 1 line
- Enable line provided for cascading (n lines to 1 line)
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT153 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT153 have two identical 4-input multiplexers which select two bits of data from up to four sources selected by common data select inputs (S₀, S₁). The two 4-input multiplexer circuits have individual active LOW output enable inputs (1 \bar{E} , 2 \bar{E}) which can be used to strobe the outputs independently. The outputs (1Y, 2Y) are forced LOW when the corresponding output enable inputs are HIGH.

The ‘153’ is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels applied to S₀ and S₁.

The logic equations for the outputs are:

$$1Y = 1\bar{E} \cdot (1I_0 \cdot \bar{S}_1 \cdot \bar{S}_0 + 1I_1 \cdot \bar{S}_1 \cdot S_0 + 1I_2 \cdot S_1 \cdot \bar{S}_0 + 1I_3 \cdot S_1 \cdot S_0)$$

$$2Y = 2\bar{E} \cdot (2I_0 \cdot \bar{S}_1 \cdot \bar{S}_0 + 2I_1 \cdot \bar{S}_1 \cdot S_0 + 2I_2 \cdot S_1 \cdot \bar{S}_0 + 2I_3 \cdot S_1 \cdot S_0)$$

The ‘153’ can be used to move data to a common output bus from a group of registers. The state of the select inputs would determine the particular register from which the data came. An alternative application is a function generator. The device can generate two functions or three variables. This is useful for implementing highly irregular random logic.

The ‘153’ is similar to the ‘253’ but has standard outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay	C _L = 15 pF; V _{CC} = 5 V			
	1I _n , 2I _n to nY		14	16	ns
	S _n to nY		15	17	ns
	n \bar{E} to nY		10	11	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per multiplexer	notes 1 and 2	30	30	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

∑ (C_L × V_{CC}² × f_o) = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

Dual 4-input multiplexer

74HC/HCT153

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\bar{E}, 2\bar{E}$	output enable inputs (active LOW)
14, 2	S_0, S_1	common data select inputs
6, 5, 4, 3	$1I_0$ to $1I_3$	data inputs from source 1
7	$1Y$	multiplexer output from source 1
8	GND	ground (0 V)
9	$2Y$	multiplexer output from source 2
10, 11, 12, 13	$2I_0$ to $2I_3$	data inputs from source 2
16	V_{CC}	positive supply voltage

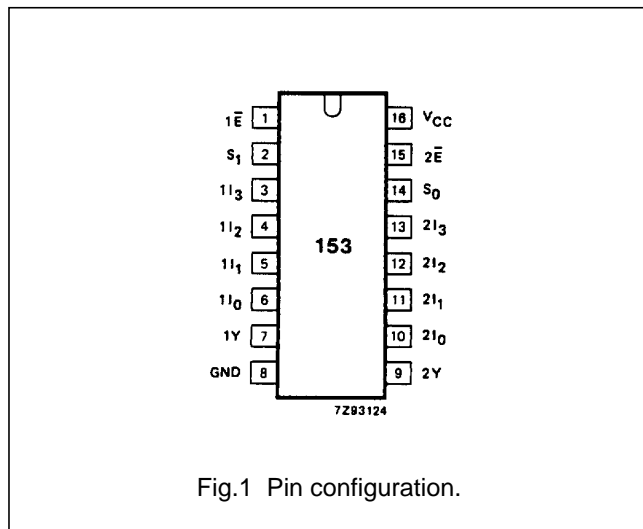


Fig.1 Pin configuration.

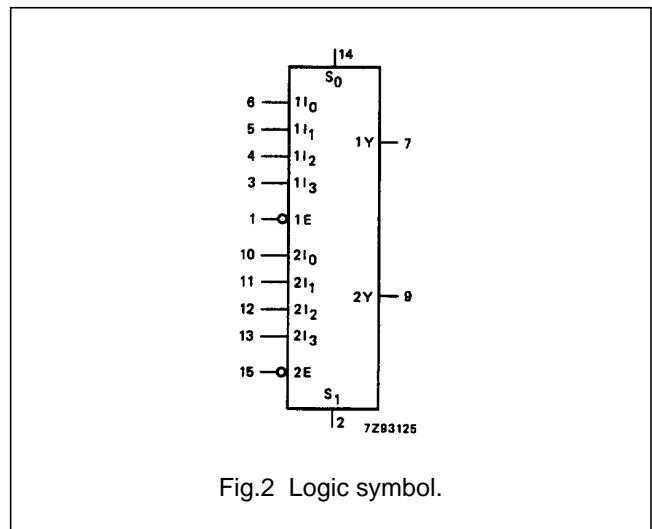


Fig.2 Logic symbol.

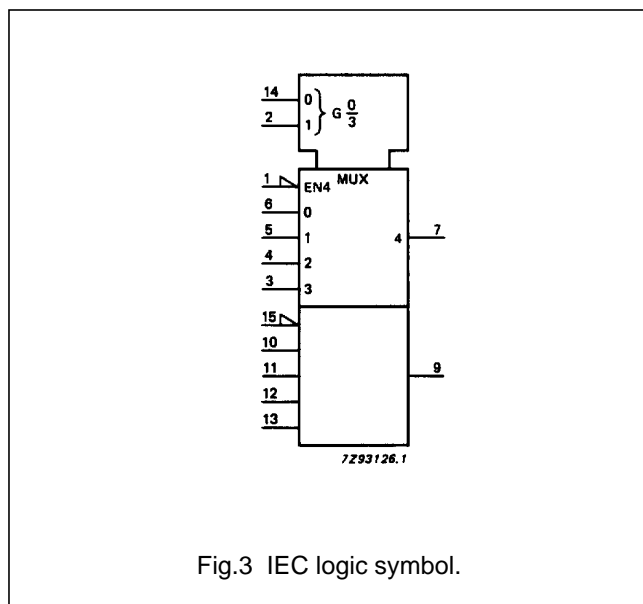


Fig.3 IEC logic symbol.

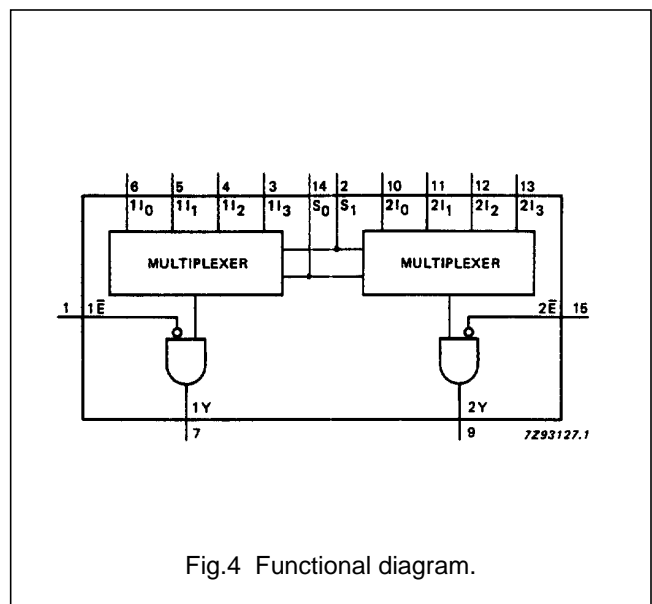


Fig.4 Functional diagram.

Dual 4-input multiplexer

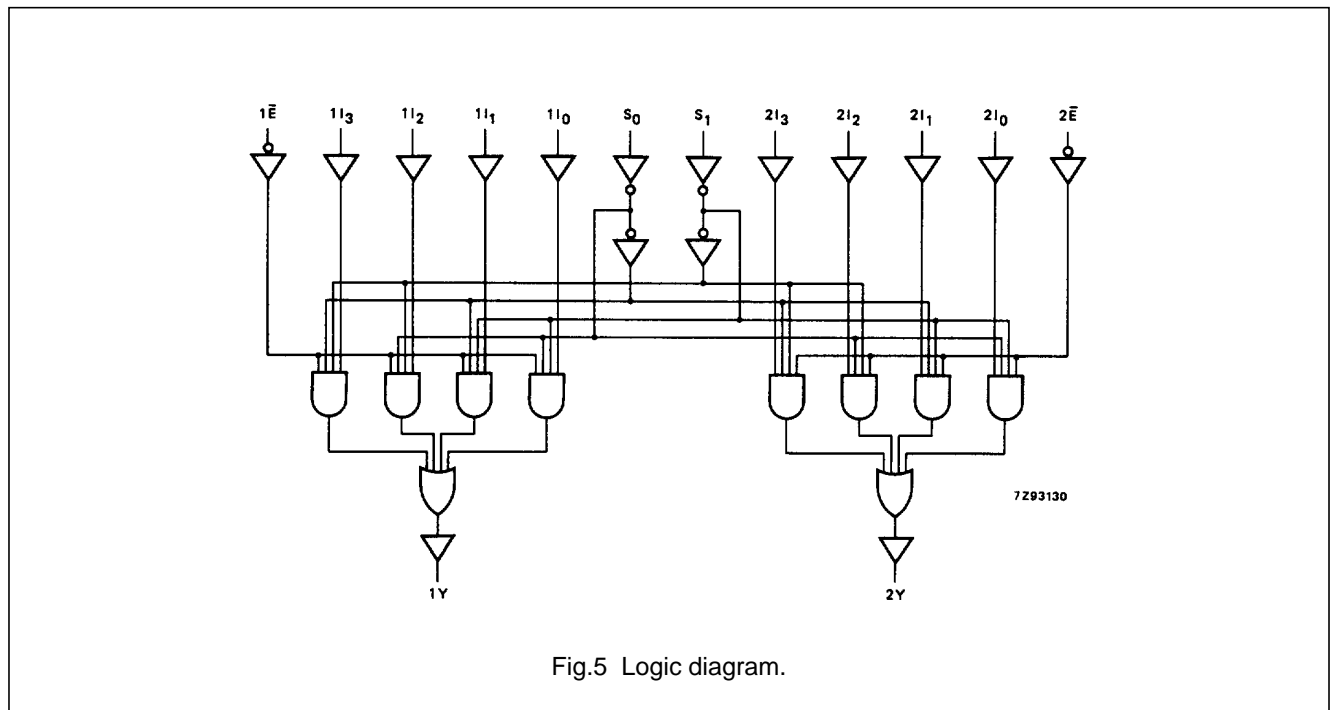
74HC/HCT153

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S ₀	S ₁	nI ₀	nI ₁	nI ₂	nI ₃	n \bar{E}	nY
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Note

- H = HIGH voltage level
L = LOW voltage level
X = don't care



Dual 4-input multiplexer

74HC/HCT153

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to+85		-40 to+125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay 1I _n to nY; 2I _n to nY		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.6
t _{PHL} / t _{PLH}	propagation delay S _n to nY		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t _{PHL} / t _{PLH}	propagation delay n \bar{E} to nY		33 12 10	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig.7
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Figs 6 and 7

Dual 4-input multiplexer

74HC/HCT153

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1I _n , 2I _n	0.45
n \bar{E}	0.60
S _n	1.35

AC CHARACTERISTICS FOR 74HCT

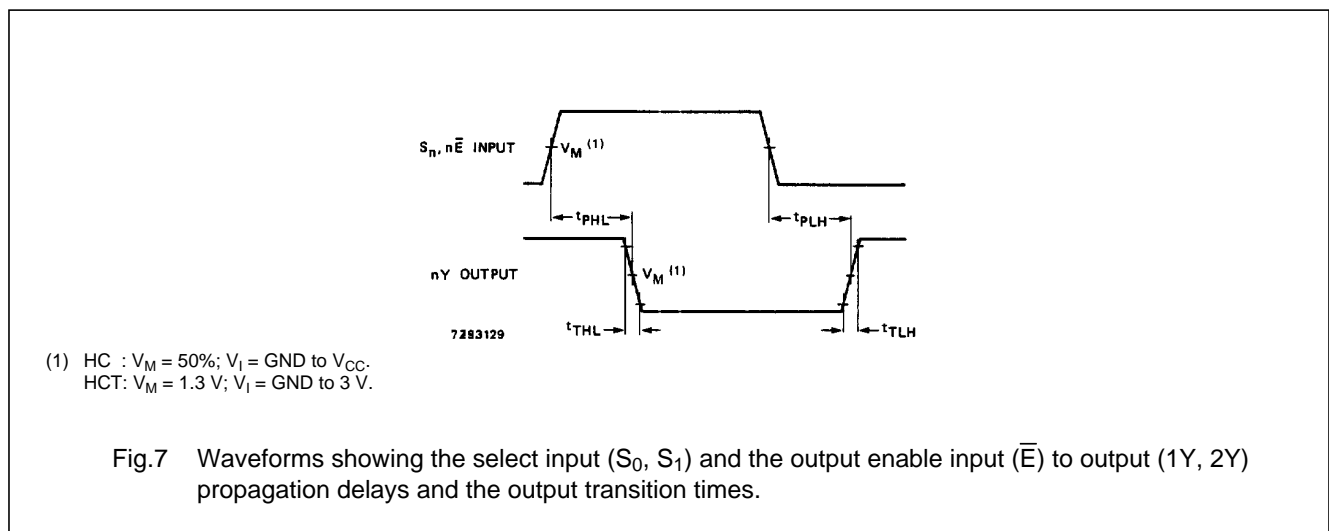
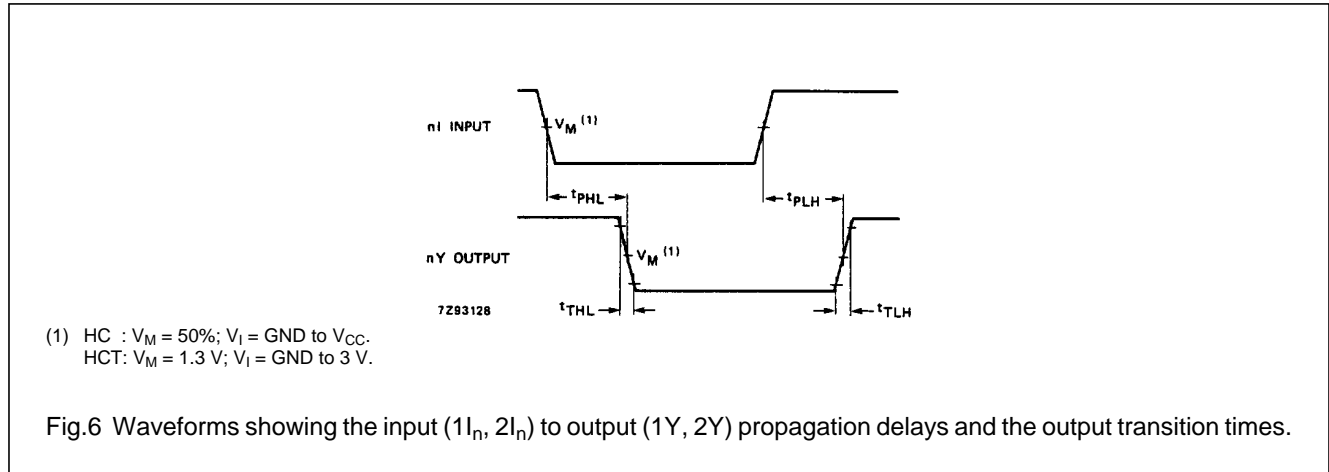
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HCT									V _{CC} (V)	WAVEFORMS
		+25			-40 to+85		-40 to+125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL}	propagation delay 1I _n to nY; 2I _n to nY		19	34		43		51	ns	4.5	Fig.6	
t _{PLH}	propagation delay 1I _n to nY; 2I _n to nY		13	24		30		36	ns	4.5	Fig.6	
t _{PHL} / t _{PLH}	propagation delay S _n to nY		20	34		43		51	ns	4.5	Fig.7	
t _{PHL} / t _{PLH}	propagation delay n \bar{E} to nY		14	27		34		41	ns	4.5	Fig.7	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7	

Dual 4-input multiplexer

74HC/HCT153

AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".