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HEF4044B

Quad R/S latch with 3-state outputs

Rev. 09 — 15 December 2009 Product data sheet

1. General description

The HEF4044B is a quad R/S latch with 3-state outputs, with a common output enable input (OE). Each latch has an active LOW set input ($1\overline{S}$ to $4\overline{S}$), an active LOW reset input ($1\overline{R}$ to $4\overline{R}$) and an active HIGH 3-state output (1Q to 4Q).

When OE is HIGH, the latch output (nQ) is determined by the $n\overline{R}$ and $n\overline{S}$ inputs as shown in Table 3. When OE is LOW, the latch outputs are in the high impedance OFF-state. OE does not affect the state of the latch. The high impedance off-state feature allows common bussing of the outputs.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input. It is also suitable for use over the industrial (−40 °C to +85 °C) temperature range.

2. Features

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Operates across the full industrial temperature range −40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

3. Applications

- Four-bit storage with output enable

4. Ordering information

Table 1. Ordering information

All types operate from −40 °C to +85 °C.

Type number	Package		
	Name	Description	Version
HEF4044BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4044BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

NXP founded by Philips

5. Functional diagram

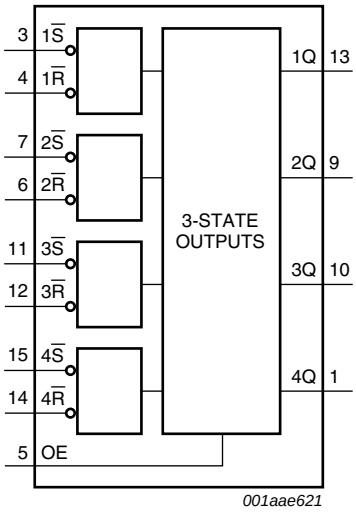

Fig 1. Functional diagram

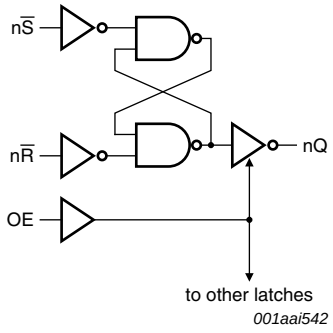

Fig 2. Logic diagram for one latch

6. Pinning information

6.1 Pinning

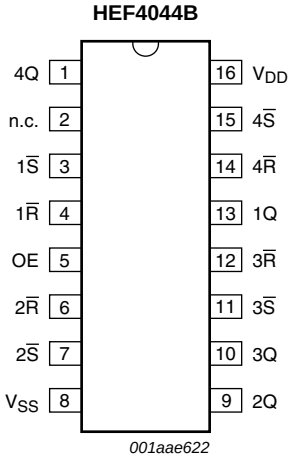

Fig 3. Pin configuration

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6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
n.c.	2	not connected
$1\overline{S}$ to $4\overline{S}$	3, 7, 11, 15	set input (active LOW)
$1\overline{R}$ to $4\overline{R}$	4, 6, 12, 14	reset input (active LOW)
OE	5	common output enable input
V_{SS}	8	ground supply voltage
1Q to 4Q	13, 9, 10, 1	3-state buffered latch output
V_{DD}	16	supply voltage

7. Functional description

Table 3. Function table[1]

Input			Output
OE	$n\overline{S}$	$n\overline{R}$	nQ
L	X	X	Z
H	L	H	H
H	X	L	L
H	H	H	latched

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high impedance state.

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V		-	±10	mA
V_I	input voltage			−0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V		-	±10	mA
$I_{I/O}$	input/output current			-	±10	mA
I_{DD}	supply current			-	50	mA
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
P_{tot}	total power dissipation	T_{amb} −40 °C to +85 °C				
		DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
		per output		-	100	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

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9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	−40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	μs/V
		V_{DD} = 10 V	-	-	0.5	μs/V
		V_{DD} = 15 V	-	-	0.08	μs/V

10. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = −40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	−1.7	-	−1.4	-	−1.1	-	mA
		V_O = 4.6 V	5 V	−0.52	-	−0.44	-	−0.36	-	mA
		V_O = 9.5 V	10 V	−1.3	-	−1.1	-	−0.9	-	mA
		V_O = 13.5 V	15 V	−3.6	-	−3.0	-	−2.4	-	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I_{OZ}	OFF-state output current	nQ output HIGH; returned to V_{DD}	15 V	-	1.6	-	1.6	-	12.0	μA
		nQ output LOW; returned to V_{SS}	15 V	-	1.6	-	1.6	-	12.0	μA

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Table 6. Static characteristics *...continued*

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = −40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
I_{DD}	supply current	I_O = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μA
			15 V	-	80	-	80	-	600	μA
C_I	input capacitance			-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C; for test circuit see Figure 6; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	$n\overline{R}$ to nQ; see Figure 4	5 V [1]	63 ns + (0.55 ns/pF)C_L	-	90	185	ns
			10 V	29 ns + (0.23 ns/pF)C_L	-	40	80	ns
			15 V	22 ns + (0.16 ns/pF)C_L	-	30	60	ns
t_{PLH}	LOW to HIGH propagation delay	$n\overline{S}$ to nQ; see Figure 4	5 V [1]	63 ns + (0.55 ns/pF)C_L	-	90	180	ns
			10 V	29 ns + (0.23 ns/pF)C_L	-	40	80	ns
			15 V	22 ns + (0.16 ns/pF)C_L	-	30	60	ns
t_t	transition time	see Figure 4	5 V [1]	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C_L	-	20	40	ns
t_{PHZ}	HIGH to OFF-state propagation delay	OE → nQ; see Figure 5	5 V		-	50	100	ns
			10 V		-	30	60	ns
			15 V		-	25	50	ns
t_{PLZ}	LOW to OFF-state propagation delay	OE → nQ; see Figure 5	5 V		-	30	60	ns
			10 V		-	25	45	ns
			15 V		-	20	40	ns
t_{PZH}	OFF-state to HIGH propagation delay	OE → nQ; see Figure 5	5 V		-	50	100	ns
			10 V		-	25	50	ns
			15 V		-	20	40	ns
t_{PZL}	OFF-state to LOW propagation delay	OE → nQ; see Figure 5	5 V		-	50	95	ns
			10 V		-	25	45	ns
			15 V		-	20	35	ns
t_W	pulse width	$n\overline{S}$ input LOW; minimum width; see Figure 4	5 V		30	15	-	ns
			10 V		20	10	-	ns
			15 V		16	8	-	ns
		$n\overline{R}$ input LOW; minimum width; see Figure 4	5 V		30	15	-	ns
			10 V		20	10	-	ns
			15 V		16	8	-	ns

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

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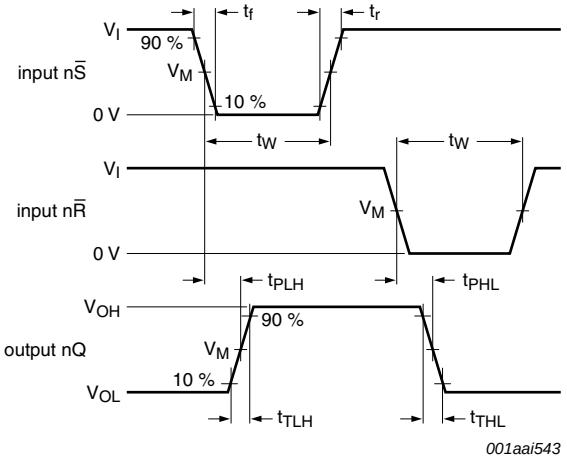
Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula for P_D (μW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 1300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz,
		10 V	$P_D = 5200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz,
		15 V	$P_D = 12900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF,
				V_{DD} = supply voltage in V,
				$\Sigma(f_o \times C_L)$ = sum of the outputs.

12. Waveforms



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. Set (nS̄) and reset (nR̄) inputs pulse width and propagation delay to latch output (nQ) and output nQ transition time

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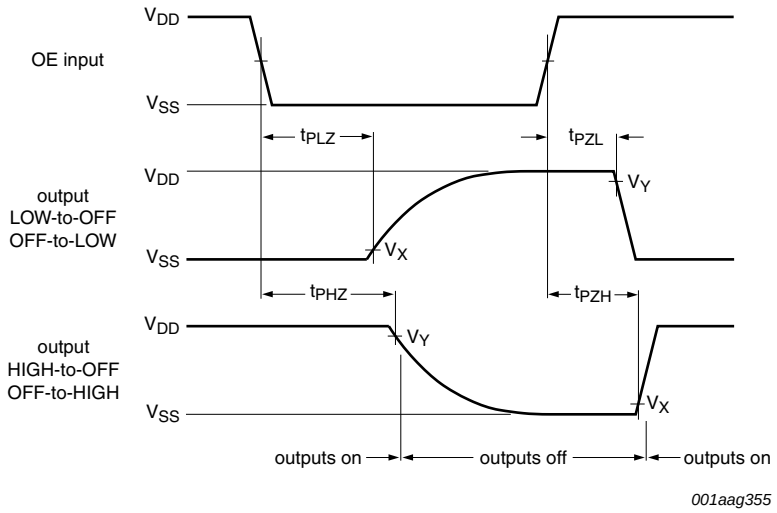

Measurement points are given in Table 9.

Fig 5. Output enable (OE) to latch output (nQ) enable time (t_{PZL} and t_{PZH}) and disable time (t_{PLZ} and t_{PHZ})

Table 9. Measurement points

Supply voltage	Input		Output		
V_{DD}	V_I	V_M	V_M	V_X	V_Y
5 V to 15 V	V_{DD} or V_{SS}	$0.5V_{DD}$	$0.5V_{DD}$	$0.1V_{DD}$	$0.9V_{DD}$

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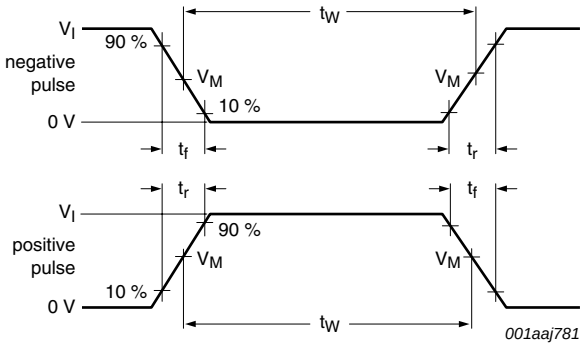
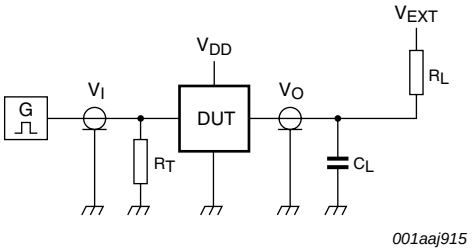


a. Input waveform



b. Test circuit

Test and measurement data is given in Table 10.

Definitions test circuit:

DUT = Device Under Test.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 6. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
5 V to 15 V	V_{DD}	≤ 20 ns	50 pF	1 kΩ	open	V_{DD}	GND

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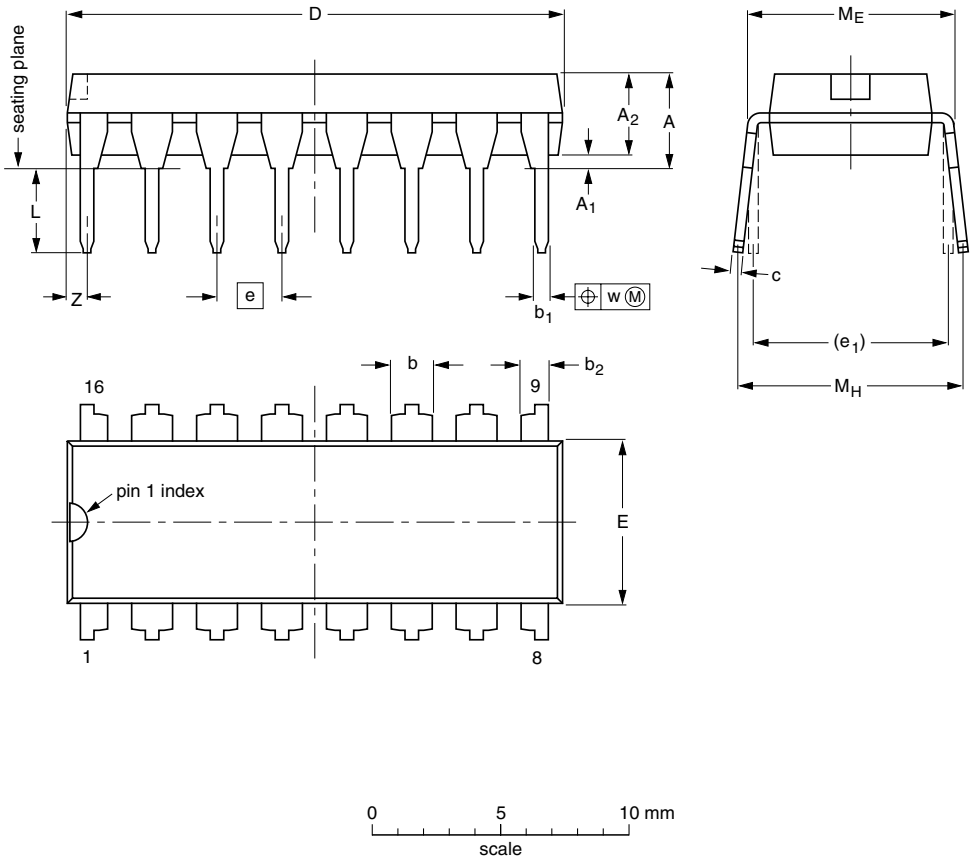
13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 7. Package outline SOT38-4 (DIP16)

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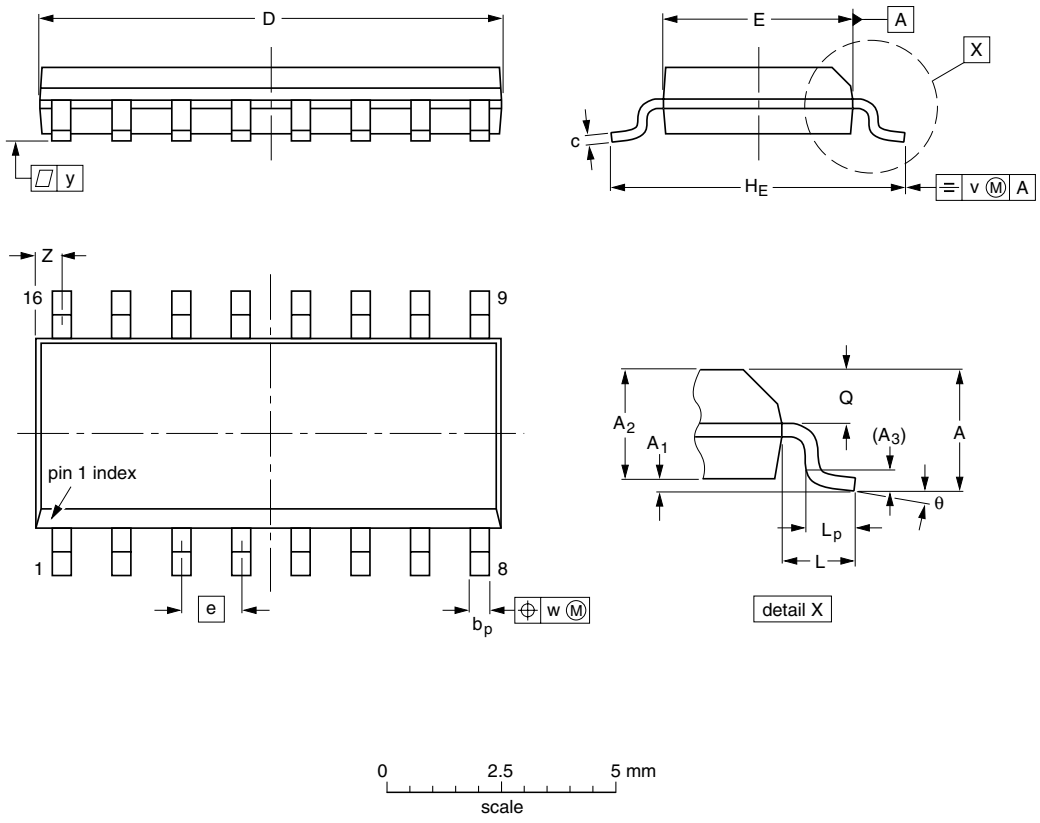
SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT109-1 (SO16)

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14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4044B_9	20091215	Product data sheet	-	HEF4044B_8
Modifications:	• Section 12 “Waveforms” Table 10 “Test data” t_{PLZ} and t_{PZL} value updated.			
HEF4044B_8	20091127	Product data sheet	-	HEF4044B_7
HEF4044B_7	20090721	Product data sheet	-	HEF4044B_6
HEF4044B_6	20081111	Product data sheet	-	HEF4044B_5
HEF4044B_5	20080812	Product data sheet	-	HEF4044B_4
HEF4044B_4	20080717	Product data sheet	-	HEF4044B_CNV_3
HEF4044B_CNV_3	19950101	Product specification	-	HEF4044B_CNV_2
HEF4044B_CNV_2	19950101	Product specification	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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