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# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT173**

**Quad D-type flip-flop; positive-edge trigger; 3-state**

Product specification  
File under Integrated Circuits, IC06

December 1990

# Quad D-type flip-flop; positive-edge trigger; 3-state

# 74HC/HCT173

## FEATURES

- Gated input enable for hold (do nothing) mode
- Gated output enable control
- Edge-triggered D-type register
- Asynchronous master reset
- Output capability: bus driver
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT173 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT173 are 4-bit parallel load registers with clock enable control, 3-state buffered outputs (Q<sub>0</sub> to Q<sub>3</sub>) and master reset (MR).

When the two data enable inputs ( $\bar{E}_1$  and  $\bar{E}_2$ ) are LOW, the data on the D<sub>n</sub> inputs is loaded into the register

synchronously with the LOW-to-HIGH clock (CP) transition. When one or both  $\bar{E}_n$  inputs are HIGH one set-up time prior to the LOW-to-HIGH clock transition, the register will retain the previous data. Data inputs and clock enable inputs are fully edge-triggered and must be stable only one set-up time prior to the LOW-to-HIGH clock transition.

The master reset input (MR) is an active HIGH asynchronous input. When MR is HIGH, all four flip-flops are reset (cleared) independently of any other input condition.

The 3-state output buffers are controlled by a 2-input NOR gate. When both output enable inputs ( $\bar{OE}_1$  and  $\bar{OE}_2$ ) are LOW, the data in the register is presented to the Q<sub>n</sub> outputs. When one or both  $\bar{OE}_n$  inputs are HIGH, the outputs are forced to a high impedance OFF-state. The 3-state output buffers are completely independent of the register operation; the  $\bar{OE}_n$  transition does not affect the clock and reset operations.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub> MR to Q <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	17	17	ns
			13	17	ns
f <sub>max</sub>	maximum clock frequency		88	88	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per flip-flop	notes 1 and 2	20	20	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

## ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2	$\overline{OE}_1, \overline{OE}_2$	output enable input (active LOW)
3, 4, 5, 6	$Q_0$ to $Q_3$	3-state flip-flop outputs
7	CP	clock input (LOW-to-HIGH, edge-triggered)
8	GND	ground (0 V)
9, 10	$\overline{E}_1, \overline{E}_2$	data enable inputs (active LOW)
14, 13, 12, 11	$D_0$ to $D_3$	data inputs
15	MR	asynchronous master reset (active HIGH)
16	$V_{CC}$	positive supply voltage

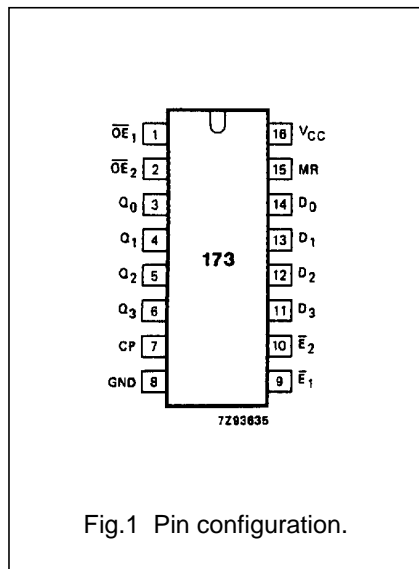


Fig.1 Pin configuration.

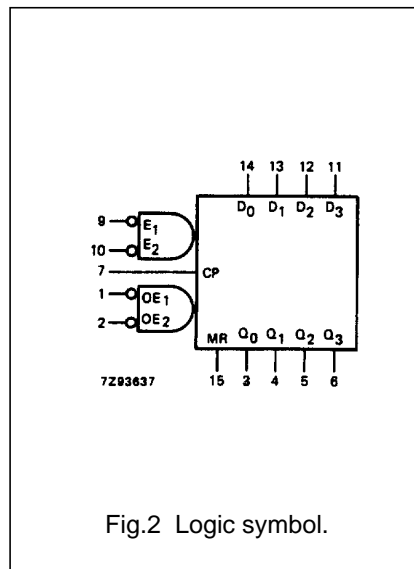


Fig.2 Logic symbol.

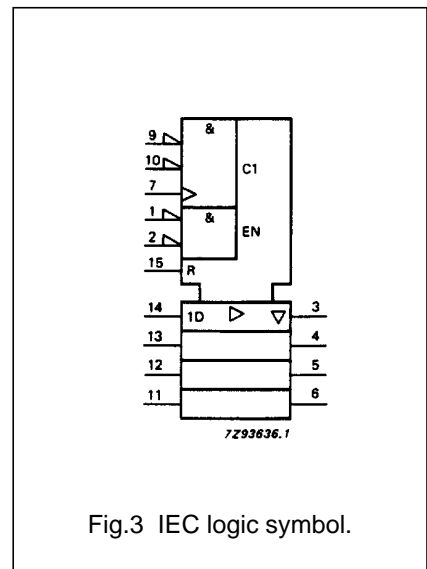


Fig.3 IEC logic symbol.

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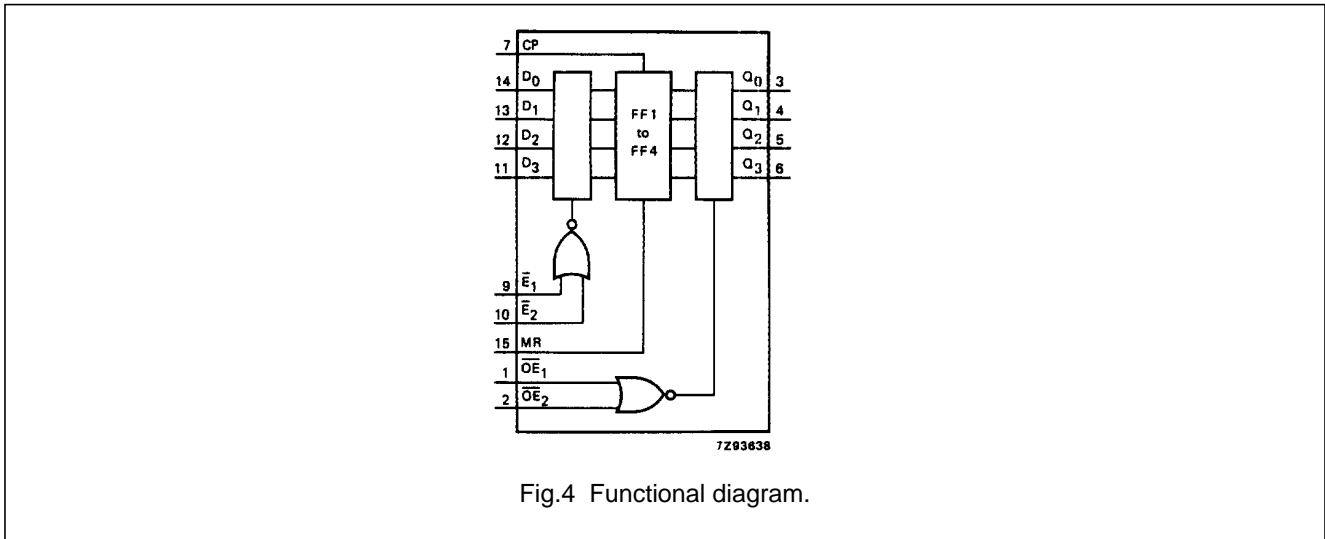


Fig.4 Functional diagram.

FUNCTION TABLE

REGISTER OPERATING MODES	INPUTS					OUTPUTS
	MR	CP	$\bar{E}_1$	$\bar{E}_2$	$D_n$	$Q_n$ (register)
reset (clear)	H	X	X	X	X	L
parallel load	L	$\uparrow$	l	l	l	L
	L	$\uparrow$	l	l	h	H
hold (no change)	L	X	h	X	X	$q_n$
	L	X	X	h	X	$q_n$

3-STATE BUFFER OPERATING MODES	INPUTS			OUTPUTS			
	$Q_n$ (register)	$\overline{OE}_1$	$\overline{OE}_2$	$Q_0$	$Q_1$	$Q_2$	$Q_3$
read	L	L	L	L	L	L	L
	H	L	L	H	H	H	H
disabled	X	H	X	Z	Z	Z	Z
	X	X	H	Z	Z	Z	Z

Notes

- H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 q = lower case letters indicate the state of the referenced input (or output)  
 one set-up time prior to the LOW-to-HIGH CP transition  
 X = don't care  
 Z = high impedance OFF-state  
 $\uparrow$  = LOW-to-HIGH CP transition

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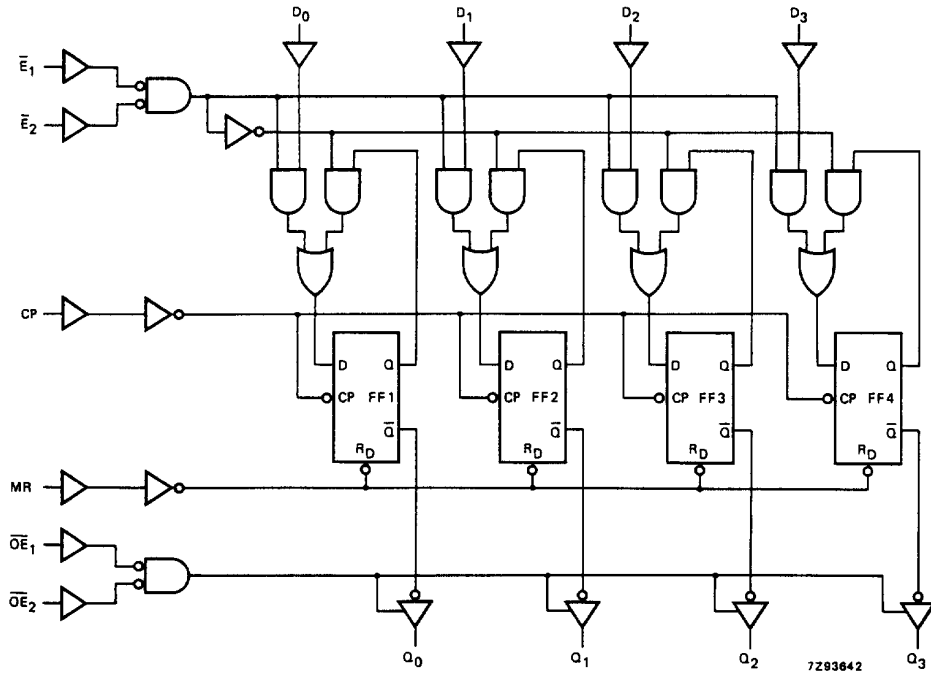


Fig.5 Logic diagram.

## Quad D-type flip-flop; positive-edge trigger; 3-state

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**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}_n$ to Q <sub>n</sub>		52 19 15	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}_n$ to Q <sub>n</sub>		52 19 15	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t <sub>w</sub>	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t <sub>w</sub>	master reset pulse width; HIGH	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t <sub>rem</sub>	removal time MR to CP	60 12 10	-8 -3 -2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.7
t <sub>su</sub>	set-up time $\overline{E}_n$ to CP	100 20 17	33 12 10		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.9
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.9

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SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS	
		74HC								V <sub>CC</sub> (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t <sub>h</sub>	hold time E <sub>n</sub> to CP	0	-17		0		0		ns	2.0 4.5 6.0	Fig.9
t <sub>h</sub>	hold time D <sub>n</sub> to CP	1	-11		1		1		ns	2.0 4.5 6.0	Fig.9
f <sub>max</sub>	maximum clock pulse frequency	6.0	26		4.8		4.0		MHz	2.0 4.5 6.0	Fig.6
		30	80		24		20				
		35	95		28		24				



## Quad D-type flip-flop; positive-edge trigger; 3-state

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**DC CHARACTERISTICS FOR 74HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{OE}_1, \overline{OE}_2$	0.50
MR	0.60
$\overline{E}_1, \overline{E}_2$	0.40
D <sub>n</sub>	0.25
CP	1.00

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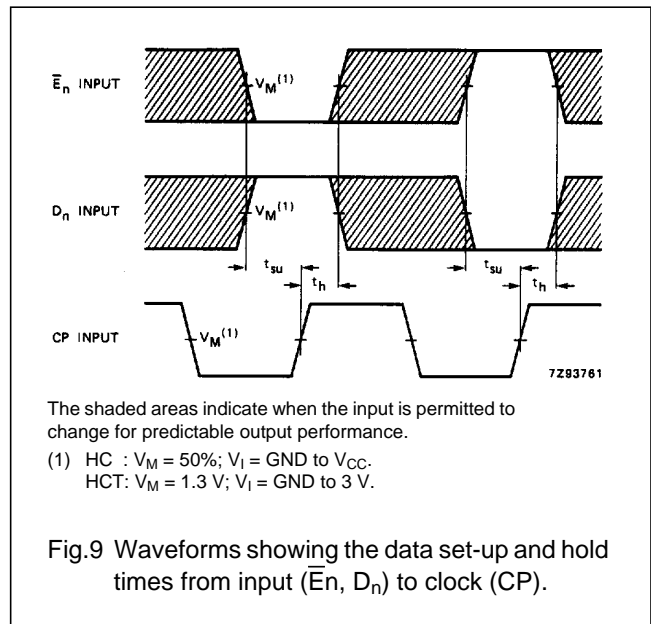
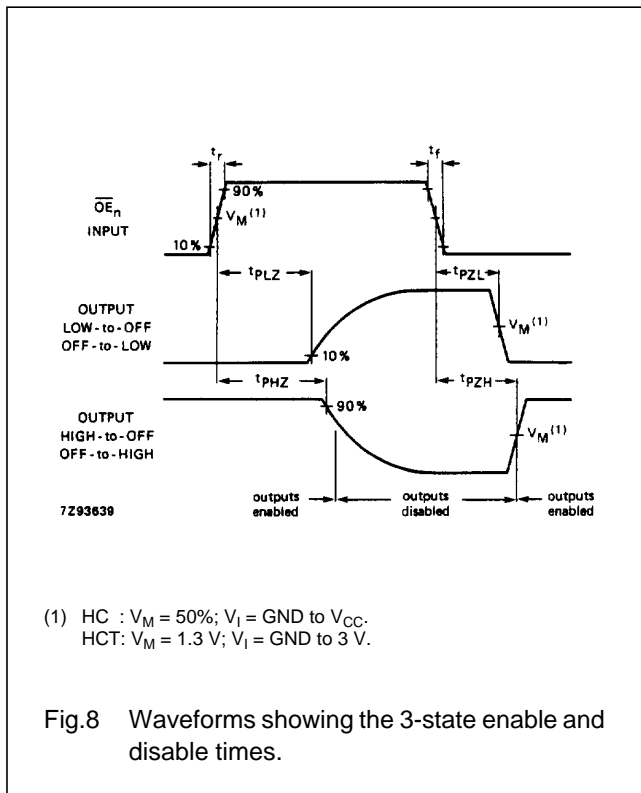
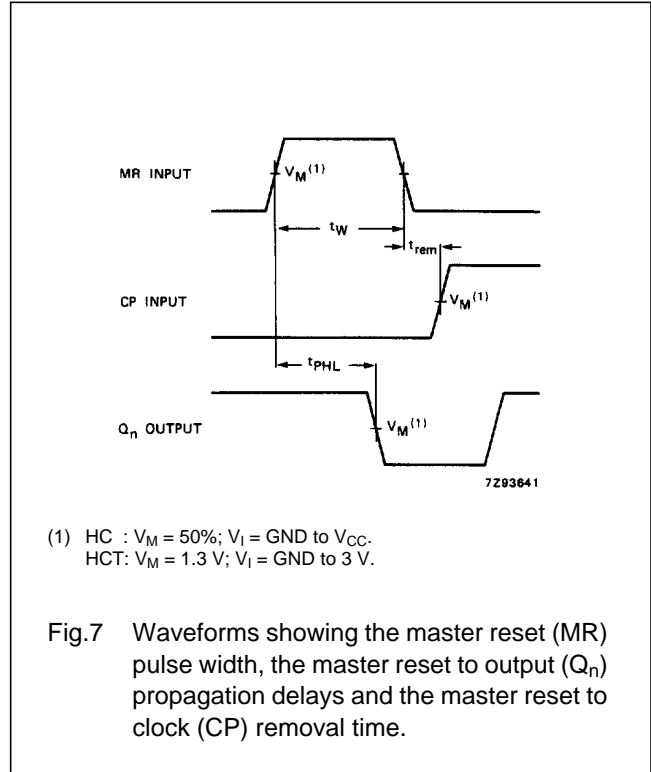
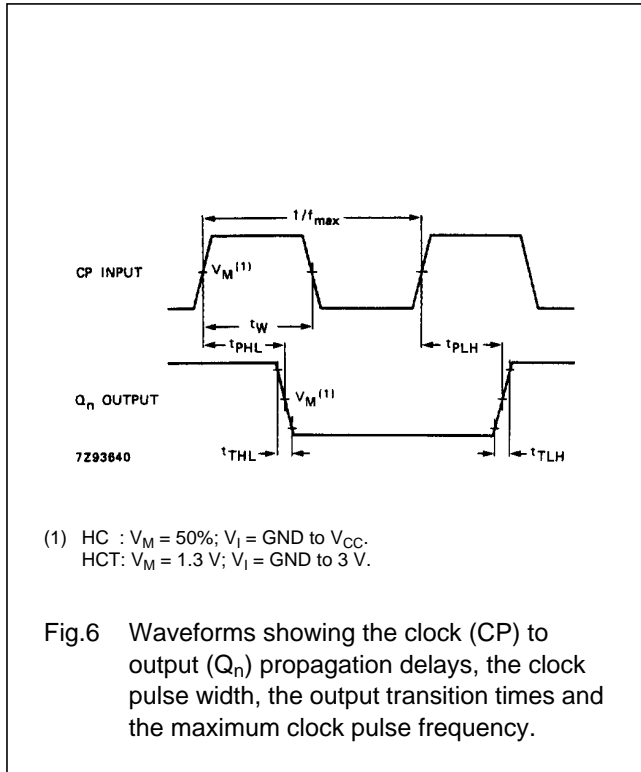
**AC CHARACTERISTICS FOR 74HCT**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		20	40		50		60	ns	4.5	Fig.6
t <sub>PHL</sub>	propagation delay MR to Q <sub>n</sub>		20	37		46		56	ns	4.5	Fig.7
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}_n$ to Q <sub>n</sub>		20	35		44		53	ns	4.5	Fig.8
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}_n$ to Q <sub>n</sub>		19	30		38		45	ns	4.5	Fig.8
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		19	ns	4.5	Fig.6
t <sub>W</sub>	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.6
t <sub>W</sub>	master reset pulse width; HIGH	15	6		19		22		ns	4.5	Fig.7
t <sub>rem</sub>	removal time MR to CP	12	-2		15		18		ns	4.5	Fig.7
t <sub>su</sub>	set-up time $\overline{E}_n$ to CP	22	13		28		33		ns	4.5	Fig.9
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	12	7		15		18		ns	4.5	Fig.9
t <sub>h</sub>	hold time $\overline{E}_n$ to CP	0	-6		0		0		ns	4.5	Fig.9
t <sub>h</sub>	hold time D <sub>n</sub> to CP	0	-3		0		0		ns	4.5	Fig.9
f <sub>max</sub>	maximum clock pulse frequency	30	80		24		20		MHz	4.5	Fig.6

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".