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## CMOS Dual Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

■ CD4098B dual monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor ( $R_X$ ) and an external capacitor ( $C_X$ ) control the timing for the circuit. Adjustment of  $R_X$  and  $C_X$  provides a wide range of output pulse widths from the Q and  $\bar{Q}$  terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of  $R_X$  and  $C_X$ .

Leading-edge-triggering (+TR) and trailing-edge-triggering (-TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to  $V_{SS}$ . An unused -TR input should be tied to  $V_{DD}$ . A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to  $V_{DD}$ . However, if an entire section of the CD4098B is not used, its RESET should be tied to  $V_{SS}$ . See Table I.

In normal operation the circuit triggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode,  $\bar{Q}$  is connected to -TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (-TR) is used.

The time period (T) for this multivibrator can be approximated by:  $T_X = \frac{1}{2} R_X C_X$  for  $C_X \geq 0.01 \mu F$ . Time periods as a function of  $R_X$  for values of  $C_X$  and  $V_{DD}$  are given in Fig. 8. Values of T vary from unit to unit and as a function of voltage, temperature, and  $R_X C_X$ .

The minimum value of external resistance,  $R_X$ , is 5 k $\Omega$ . The maximum value of external capacitance,  $C_X$ , is 100  $\mu F$ . Fig. 9 shows time periods as a function of  $C_X$  for values of  $R_X$  and  $V_{DD}$ .

The output pulse width has variations of  $\pm 2.5\%$  typically, over the temperature range of  $-55^\circ C$  to  $125^\circ C$  for  $C_X = 1000$  pF and  $R_X = 100$  k $\Omega$ .

For power supply variations of  $\pm 5\%$ , the output pulse width has variations of  $\pm 0.5\%$  typically, for  $V_{DD} = 10$  V and 15 V and  $\pm 1\%$  typically, for  $V_{DD} = 5$  V at  $C_X = 1000$  pF and  $R_X = 5$  k $\Omega$ .

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

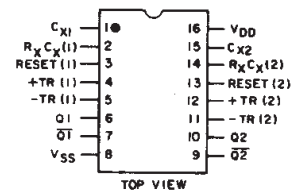
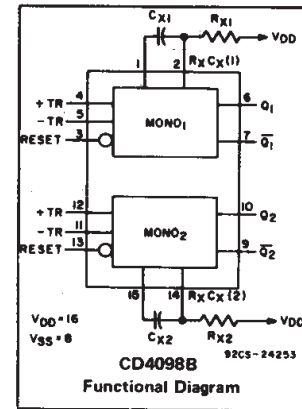
The CD4098B is similar to type MC14528.

### Features:

- Retriggerable/resettable capability
- Trigger and reset propagation delays independent of  $R_X$ ,  $C_X$
- Triggering from leading or trailing edge
- Q and  $\bar{Q}$  buffered outputs available
- Separate resets
- Wide range of output-pulse widths
- 100% tested for maximum quiescent current at 20 V
- Maximum input current of 1  $\mu A$  at 18 V over full package-temperature range; 100 nA at 18 V and  $25^\circ C$
- Noise margin (full package-temperature range):
  - 1 V at  $V_{DD} = 5$  V
  - 2 V at  $V_{DD} = 10$  V
  - 2.5 V at  $V_{DD} = 15$  V
- 5-V, 10-V, and 15-V parametric ratings
- Standardized, symmetrical output characteristics
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices."

### Applications:

- Pulse delay and timing
- Pulse shaping
- Astable multivibrator



TERMINALS 1, 8, 15 ARE ELECTRICALLY CONNECTED INTERNALLY  
92CS-24848RI  
**TERMINAL ASSIGNMENT**

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	Voltages referenced to $V_{SS}$ Terminal)		-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS			-0.5V to $V_{DD} + 0.5V$
DC INPUT CURRENT, ANY ONE INPUT			$\pm 10$ mA
POWER DISSIPATION PER PACKAGE ( $P_D$ ):			
For $T_A = -55^\circ C$ to $+100^\circ C$			500mW
For $T_A = +100^\circ C$ to $+125^\circ C$	Derate Linearly at 12mW/ $^\circ C$		to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR			
For $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)			100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )			$-55^\circ C$ to $+125^\circ C$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )			$-85^\circ C$ to $+150^\circ C$
LEAD TEMPERATURE (DURING SOLDERING):			
At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79mm) from case for 10s max			$+265^\circ C$

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	$V_{DD}$ V	LIMITS		UNITS
		MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)	-	3	18	V
Trigger Pulse Width $t_W(TR)$	5 10 15	140 60 40	- - -	ns
Reset Pulse Width $t_W(R)$ (This is a function of $C_X$ )	-	See Dynamic Char. Chart and Fig. 10		-
Trigger Rise or Fall Time $t_r(TR)$ , $t_f(TR)$	5 - 15	-	100	$\mu s$

# CD4098B Types

TABLE I

CD4098B FUNCTIONAL TERMINAL CONNECTIONS

FUNCTION	V <sub>DD</sub> TO TERM. NO.		V <sub>SS</sub> TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>	MONO <sub>1</sub>	MONO <sub>2</sub>
Leading-Edge Trigger/Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/Non-retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/Non-retriggerable	3	13			5	11	4-6	12-10
Unused Section	5	11	3, 4	12, 13				

NOTES:

1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS AN OUTPUT PULSE WIDTH WHICH IS EXTENDED ONE FULL TIME PERIOD (T<sub>X</sub>) AFTER APPLICATION OF THE LAST TRIGGER PULSE.

The minimum time between retriggering edges (or trigger and retrigger edges) is 40 per cent of (T<sub>X</sub>).

2. A NON-RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD T<sub>X</sub> REFERENCED FROM THE APPLICATION OF THE FIRST TRIGGER PULSE.

INPUT PULSE TRAIN



RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)



NON-RETRIGGERABLE MODE PULSE WIDTH (+TR MODE)

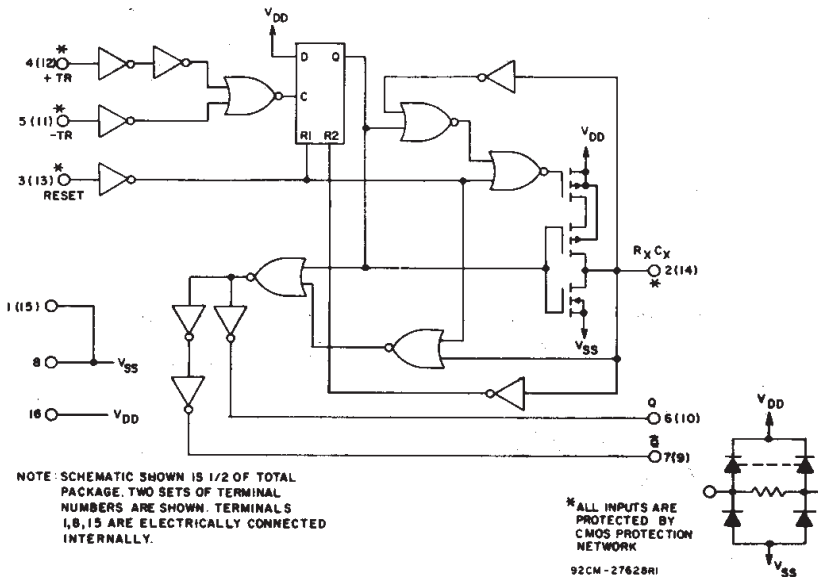
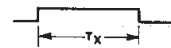


Fig. 4 - CD4098B logic diagram.

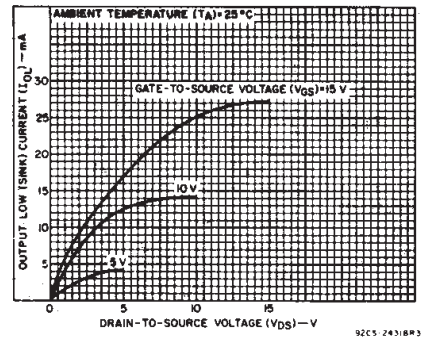


Fig. 1 - Typical output low (sink) current characteristics.

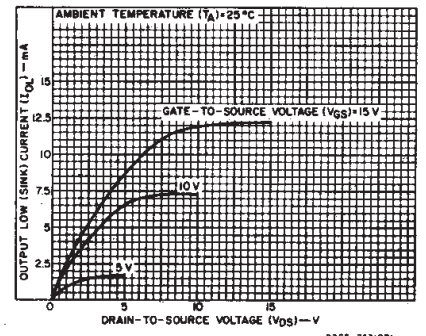


Fig. 2 - Minimum output low (sink) current characteristics.

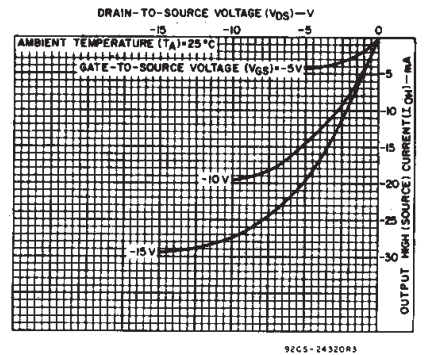


Fig. 3 - Typical output high (source) current characteristics.

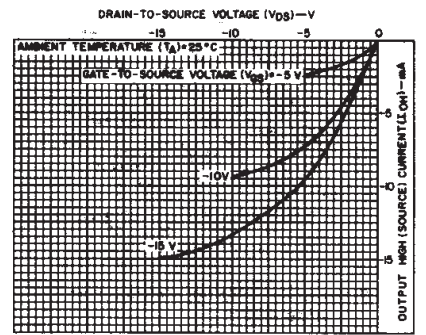


Fig. 5 - Minimum output high (source) current characteristics.

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# CD4098B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current	—	0.5	5	1	1	30	30	—	0.02	1	μA
I <sub>DD</sub> Max.	—	0.10	10	2	2	60	60	—	0.02	2	
I <sub>DD</sub> Max.	—	0.15	15	4	4	120	120	—	0.02	4	
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
I <sub>OL</sub> Min.	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
I <sub>OL</sub> Min.	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
I <sub>OH</sub> Min.	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
I <sub>OH</sub> Min.	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0.5	5	0.05			—			0	V
V <sub>OL</sub> Max.	—	0.10	10	0.05			—			0	
V <sub>OL</sub> Max.	—	0.15	15	0.05			—			0	
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0.5	5	4.95			4.95			5	V
V <sub>OH</sub> Min.	—	0.10	10	9.95			9.95			10	
V <sub>OH</sub> Min.	—	0.15	15	14.95			14.95			15	
Input Low Voltage, V <sub>IL</sub> Max.	0.5, 4.5	—	5	1.5			—			1.5	V
V <sub>IL</sub> Max.	1.9	—	10	3			—			3	
V <sub>IL</sub> Max.	1.5, 13.5	—	15	4			—			4	
Input High Voltage, V <sub>IH</sub> Min.	0.5, 4.5	—	5	3.5			3.5			—	V
V <sub>IH</sub> Min.	1.9	—	10	7			7			—	
V <sub>IH</sub> Min.	1.5, 13.5	—	15	11			11			—	
Input Current, I <sub>IN</sub> Max.	—	0.18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA
Output Leakage I <sub>OUT</sub> Max.	0.18	0.18	18	±0.4	±0.4	±12	±12	—	±10 <sup>-4</sup>	±0.4	μA

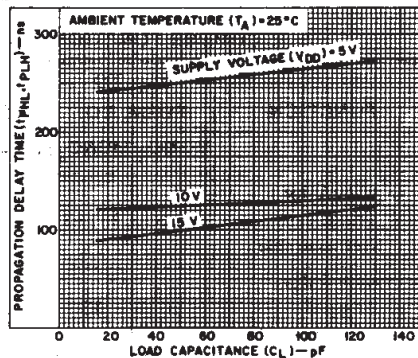


Fig. 6 - Typical propagation delay time vs. load capacitance, trigger into Q out. (All values of C<sub>X</sub> and R<sub>X</sub>.)

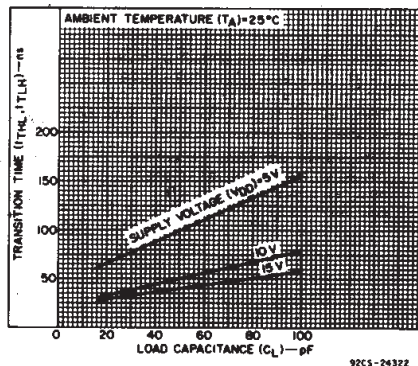


Fig. 7 - Transition time vs. load capacitance for R<sub>X</sub> = 5 kΩ-10000 kΩ and C<sub>X</sub> = 15 pF-10000 pF.

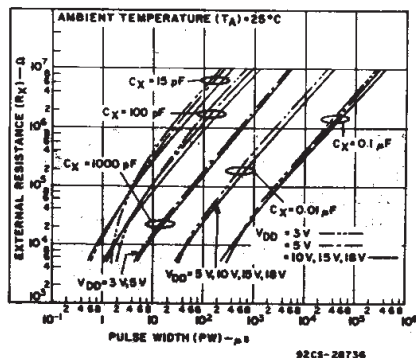


Fig. 8 - Typical external resistance vs. pulse width.

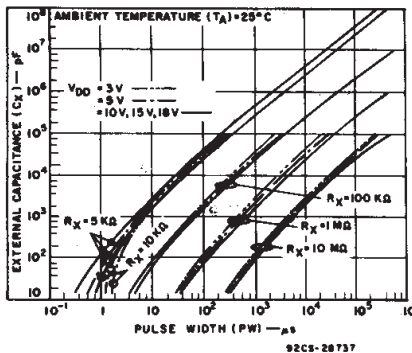


Fig. 9 - Typical external capacitance vs. pulse width.

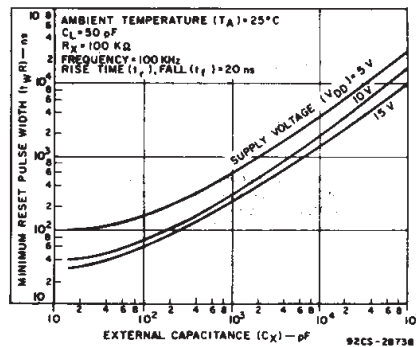


Fig. 10 - Typical minimum reset pulse width vs. external capacitance.

# CD4098B Types

## DYNAMIC ELECTRICAL CHARACTERISTICS

At  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS			LIMITS		UNITS
	$R_X$ (k $\Omega$ )	$C_X$ (pF)	$V_{DD}$ (V)	Typ.	Max.	
Trigger Propagation Delay Time +TR, -TR to Q, $\bar{Q}$ $t_{PHL}$ , $t_{PLH}$	5 to 10,000	$\geq 15$	5 10 15	250 125 100	500 250 200	ns
Minimum Trigger Pulse Width, $t_{WH}$ , $t_{WL}$	5 to 10,000	$\geq 15$	5 10 15	70 30 20	140 60 40	ns
Transition Time, $t_{TLH}$	5 to 10,000	$\geq 15$	5 10 15	100 50 40	200 100 80	ns
$t_{THL}$	5 to 10,000	15 to 10,000	5 10 15	100 50 40	200 100 80	
	5 to 10,000	0.01 $\mu\text{F}$ to 0.1 $\mu\text{F}$	5 10 15	150 75 65	300 150 130	
	5 to 10,000	0.1 $\mu\text{F}$ to 1 $\mu\text{F}$	5 10 15	250 150 80	500 300 160	
Reset Propagation Delay Time, $T_{PHL}$ , $T_{PLH}$	5 to 10,000	$\geq 15$	5 10 15	225 125 75	450 250 150	ns
Minimum Reset Pulse Width, $t_{WR}$	100	15	5 10 15	100 40 30	200 80 60	ns
		1000	5 10 15	600 300 250	1200 600 500	
		0.1 $\mu\text{F}$	5 10 15	25 15 10	50 30 20	$\mu\text{s}$
Trigger Rise or Fall Time $t_r$ (TR), $t_f$ (TR)	—	—	5 to 15	—	100	$\mu\text{s}$
Pulse Width Match Between Circuits in Same Package	10	10,000	5 10 15	5 7.5 7.5	10 15 15	%
Input Capacitance, $C_{iN}$	Any Input			5	7.5	pF

## TEST CIRCUITS

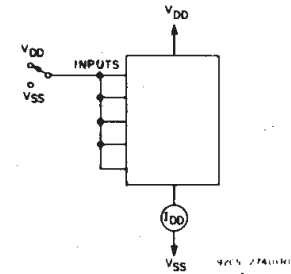


Fig. 12 - Quiescent-device-current test circuits.

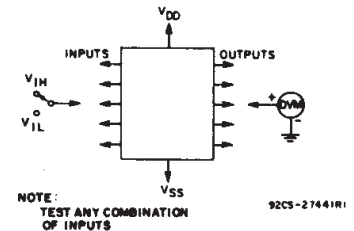


Fig. 13 - Input-voltage test circuit.

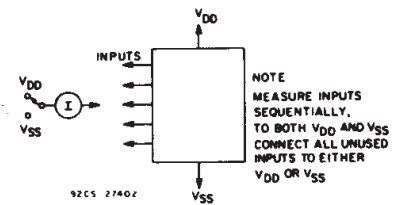


Fig. 14 - Input leakage current test circuit.

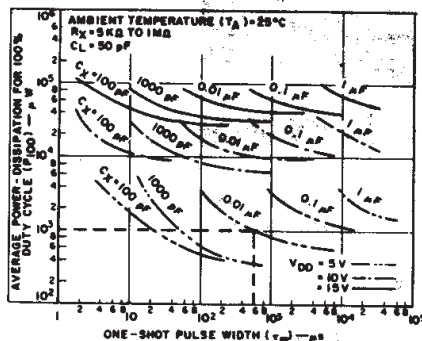
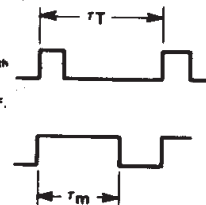


Fig. 11 - Average power dissipation vs. one-shot pulse width.

To calculate average power dissipation ( $P$ ) for less than 100% duty cycle:  
 $P_{100}$  = average power for 100% duty cycle  
 $P = \left(\frac{\tau_m}{T_T}\right) P_{100}$  where  $\tau_m$  = one-shot pulse width  
 $T_T$  = trigger pulse period

e.g. For  $\tau_m = 600\ \mu\text{s}$ ,  $T_T = 1000\ \mu\text{s}$ ,  $C_X = 0.01\ \mu\text{F}$ ,  
 $V_{DD} = 5\text{ V}$   
 $P = \left(\frac{600}{1000}\right) 10^{-3} = 600\ \mu\text{W}$  (see dotted line on graph)



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# CD4098B Types

## APPLICATIONS

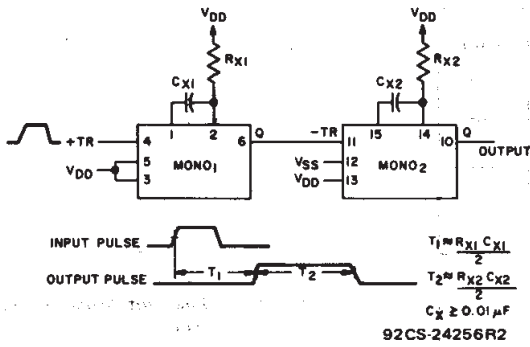


Fig. 15 - Pulse delay.

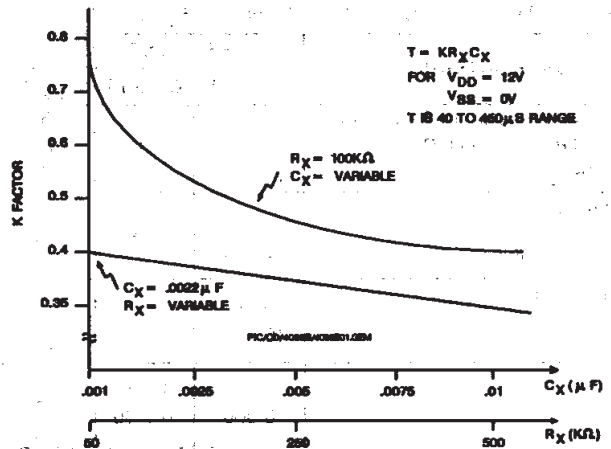


Fig. 17 - K-Factor for  $V_{DD} = 12V$ .

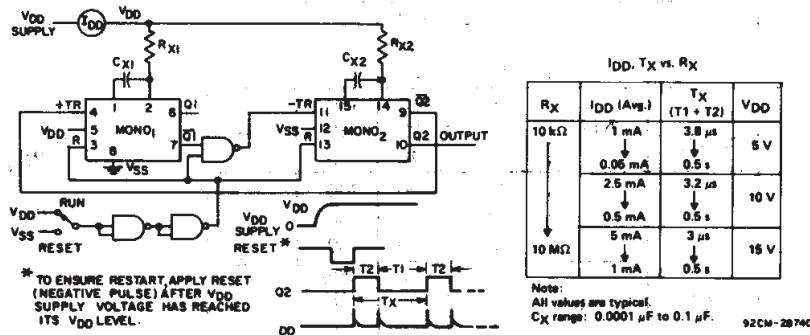
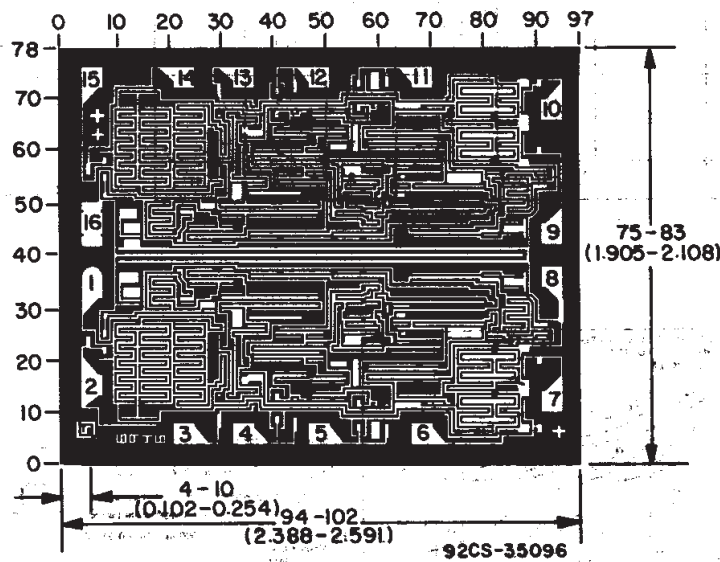


Fig. 16 - Astable multivibrator with restart after reset capability.

IDD, T\_X vs. R\_X

$R_X$	$I_{DD}$ (Avg.)	$T_X$ ( $T_1 + T_2$ )	$V_{DD}$
10 k $\Omega$	1 mA	3.8 $\mu s$	5 V
	0.05 mA	0.5 s	
10 M $\Omega$	2.5 mA	3.2 $\mu s$	10 V
	0.5 mA	0.5 s	
10 M $\Omega$	5 mA	3 $\mu s$	15 V
	1 mA	0.5 s	

Note:  
 All values are typical.  
 $C_X$  range: 0.0001  $\mu F$  to 0.1  $\mu F$ .  
 92CM-28740



### Dimensions and Pad Layout for CD4098BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

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