Features

- System-on-chip technology to handle all ground link communication
- Can be operated independently from a processor
- Re-definable by the use of different mission PROM
- Supports multiple sources of CPDU segments
- Packet wire or Space Wire control interface for all chip accesses
- Can use either 8- or 16-bit PROM and RAM
- 3.3V supply voltage
- Operating frequency :16 MHz
- Maximum frequency : 22.2 MHz
- Technology MH1RT 0.35µm - 4 metal layers - Sea of gates.
  - Radiation Hardened CMOS process
  - No single event latch-up below a LET threshold of 70 MeV/mg/cm
  - SEU hardened flip-flops
  - Functional and parametric total dose capability up to 200 krads (Si).
- Package : 256-pin QFP package.
- Quality flows : Military and Space level B according to Atmel quality flow document reference 4288

Single Chip Telemetry and Telecommand

AT7909E

1. Description

The AT7909E is an integrated device providing on-board telemetry and telecommand services via standardized interfaces.

The AT7909E is mainly an integrated telecommand decoder and telemetry encoder device. It can operate in stand-alone mode, without requiring any programming or support from an on-board computer. It can also operate in tight integration with a computer, featuring fast communication links for both commanding and data transfer. The different capabilities of the AT7909E can work together, or separately when only part of the functionality is required in a system, e.g. a telecommand decoder or telemetry encoder only.

The AT7909E was designed by Saab Space, Sweden (ESTEC / contract no. 16064/02/NL/FM), who will bring the technical answers to all questions relative to functionality through Atmel hot line assp-applab.hotline@nto.atmel.com.

This document shall be read in conjunction with Saab Space 'SCTMTC ASIC user's manual reference P-ASIC-NOT-00122-SE'.

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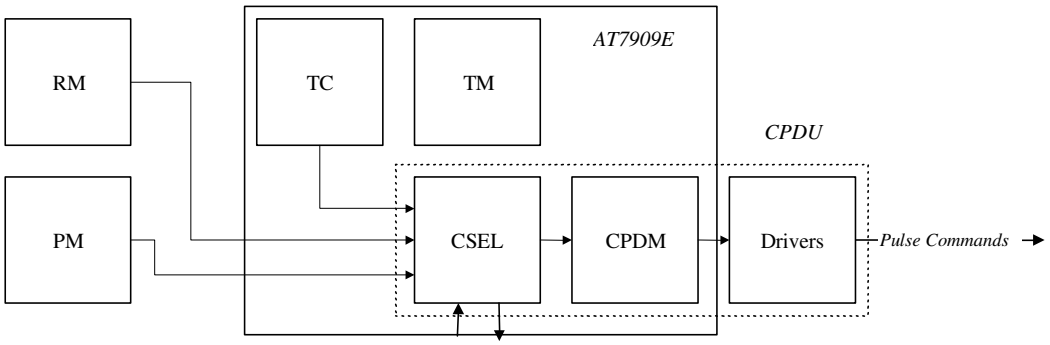
2. System Overview

AT7909E has been designed with a generic system architecture in mind. This architecture is assumed to consist of certain elements, although this is not a requirement for successful usage of the device.

The main elements in this architecture are:

- Processor Module (PM)
  Comprising a processor or similar unit that is in control of the AT7909E. A PM communicates with the AT7909E by means of serial control interfaces.
  Dedicated serial interfaces are used for the reception of telecommands and transmission of telemetry from the PM. A PM is, however, not needed to control AT7909E, since AT7909E is autonomous.
- Reconfiguration Module (RM)
  Comprising an autonomous unit, possibly a processor, which is allowed to send sequences of command instructions to the CPDU described hereafter.
- Telecommand Decoder (TC)
  Comprising the Packet Telecommand Decoder (PDEC3) which is integrated in the AT7909E.
- Command Pulse Distribution Unit (CPDU)
  Comprising the Command Pulse Distribution (CPDM) and Selector (CSEL) modules integrated in the AT7909E, as well as a set of external high and low power drivers implemented by the user.
- Telemetry Encoder (TM)
  Comprising the Packet Telemetry Encoder (TME) which is integrated in the AT7909E.

Figure 2-1. AT7909E System block diagram



PM acronym is used to indicate any unit that can access the Internal Bus of the AT7909E. This might be done via the SpaceWire interface or the Control Interface Module.

An RM is not part of the AT7909E, but the acronym is used to indicate an external unit that can be connected to the CPDU via the External CPDU Interfaces. The CPDU handles such units in a special manner that will be explained when describing the CSEL module.

The acronym TC generally refers to the on-chip PDEC3 telecommand decoder. However, the CPDU has a specific TC request interface that is handled in a special manner that is explained in the description of the CSEL module. This interface can also be connected to the External CPDU Interface if required

3. Functions

The Single Chip Telemetry and Telecommand AT7909E has the following functions:

- Test Access Port
  The AT7909E includes an IEEE® standard 1149.1 [JTAG] TAP block, which can be used for manufacturing test of printed circuit boards on which the AT7909E is mounted.
- Clock and Reset block
  This block ensures that there is a clock of the correct frequency for each block and module in the AT7909E. The block also generates the reset signal to each block and module in the AT7909E. The block includes a reset register, which can be used to reset some of the modules in the AT7909E.
- Configuration block
  The Configuration block will after power-up configure the AT7909E according to the mission PROM, i.e. setup SpaceWire source clock, TME frame length etc. The Configuration block can also make a continuos refresh of all or part of the configuration registers inside AT7909E.
- Memory Interface
  The memory interface supports SRAM and PROM and provides EDAC protection of the memory. The EDAC corrects single bit errors and detects double bit errors. The memory interface also includes a scrubber.
- Packet Telecommand Decoder [PDEC3]
  The telecommand decoder is fully compliant with ESA and CCSDS standards, specifications and recommendations. In addition, a Command Pulse Distribution Unit (CPDU) is composed of the CPDM, CSEL and ExtCpduIf described hereafter.
- External Command Pulse Distribution Unit Interface [ExtCpduIf]
  The ExtCpduIf provides a way for an external unit to generate command pulses using the internal CPDM. The input interface is based on the Packet Wire protocol including ready and abort signals.
- Command Pulse Distribution Selector [CSEL]
  The CSEL arbitrates access to the CPDM between three input request sources: the Reconfiguration Module (RM), the Telecommand Decoder (TC), and the Processor Module (PM). CSEL arbitrates between the input request sources, while CPDM executes the command sequence from the source that has been selected. The CSEL module includes a status interface, which ensures that the nominal and redundant CPDUs in a system are not interrupting each other.
- Command Pulse Distribution Module [CPDM]
  The CPDM receives telecommand segments on which it performs clean and legal checks. Each command instruction contained in the telecommand segment will result in an output pulse being generated for a specified time duration.
- Packet Telemetry Encoder [TME]
  The telemetry encoder and telemetry channel encoder are fully compliant with ESA and CCSDS standards and recommendations. The telemetry encoder physically implements eight Virtual Channels, which are named A to H.
- SpaceWire [SPW]
  The SpaceWire interface can be configured for transfer of data to one or several telemetry encoder Virtual Channels. The routing is done using the header of the SpaceWire packet. The SpaceWire interface can also be used for configuring the AT7909E.

- Control Interface Module [CI]
  The Control Interface Module provides a connection between external serial interfaces to the internal bus of the AT7909E to allow an external PM to control and configure the device. The CI is connected to the SpaceWire interface described above and to a serial Packet Wire interface dedicated for control.

4. Interfaces

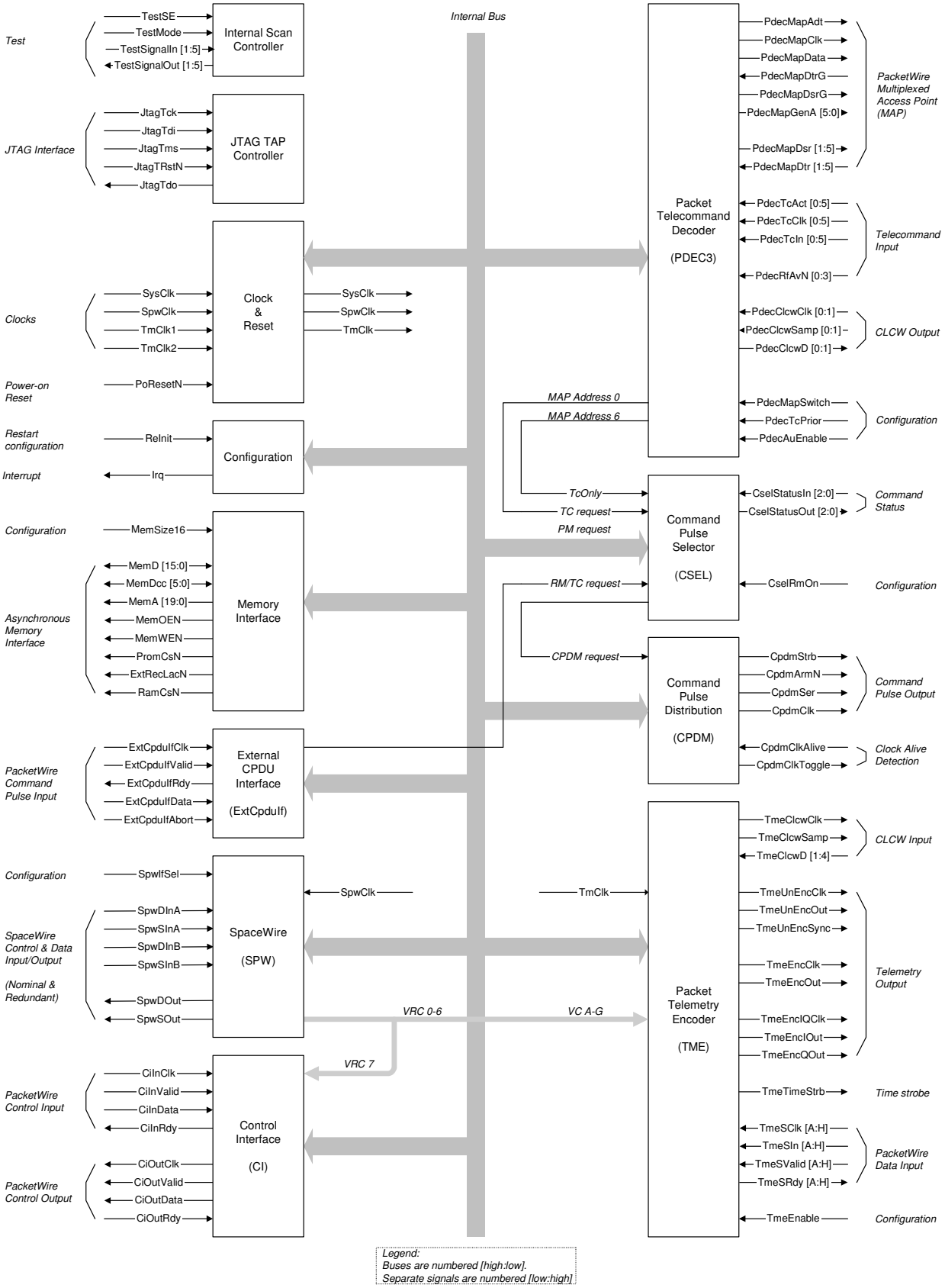
The AT7909E has the following interfaces:

- IEEE 1149.1 TAP interface
- Clock and Reset
  Separate clock inputs for system, telemetry and SpaceWire bit rates.
- Memory Interface
  - Support for 8 or 16 bit wide data bus, with optional EDAC protection.
  - Support for SRAM and PROM.
- Packet Telecommand Decoder
  - Six separate serial telecommand input streams.
  - Four RF available status inputs.
  - Two external interfaces allowing readout of the CLCW. The internal Packet Telemetry Encoder is connected via one of these external interfaces if used.
  - Five dedicated, i.e. internally decoded, and one general serial MAP interface providing the accepted Telecommand Segments. Each dedicated MAP interface has separate Terminal and Sender Ready pins. All MAP interfaces share the clock, data and abort signals.
  - AU enable/disable selection.
  - Enable/disable for priority selection of telecommand input streams.
- External CPDU Interface
  Packet Wire based interface for receiving telecommand segments bound for the internal CPDU function
- Command Pulse Distribution Unit
  - Command pulse output interface
  - Clock alive detection interface
  - Remote CPDU status interface, to communicate with a redundant CPDU
  - External setting of operating mode
- Packet Telemetry Encoder
  - Eight Packet Wire interfaces for telemetry input.
  - Four external interfaces for retrieval of the CLCW from Packet Telecommand Decoders. The interfaces have separate data input but share control signals.
  - Telemetry Transfer Frame output interfaces: unencoded, encoded and modulated. All interfaces are serial bit stream with an associated clock. Except for the unencoded output, there are five different formats: PSK Squarewave, NRZ-L, NRZ-M, SP-L and I/Q. The five share the same interface. In addition, the unencoded output also has the *TmeUnEncSync* signal that is asserted while each and every Attached Synchronisation Marker is output.

  - A strobe to allow the on-board time to be sampled synchronously with the generated Transfer Frames, named *TmeTimeStrb*.

- SpaceWire interface (nominal and redundant)
  For data transfers to the Telemetry Encoder (TME) and for communication with the Control Interface Module (CI) for control and configuration of the AT7909E.
- Packet Wire interface (receive and transmit)
  For communication with the Control Interface Module (CI) for control and configuration of the AT7909E.

5. AT7909E Block diagram



6. Signal pins description

The AT7909E inputs and outputs are as defined in the tables below. For each signal, the type is indicated (CMOS, Schmitt). For each output signal, the drive strength is indicated (LD/MD/HD = Low/Mid/High Drive). PD stands for Pull-Down, and PDL stands for Pull-Down Low resistance. Clock in the rightmost column is the name of the reference clock if the signal is synchronous.

6.1 General AT7909E signals

Table 6-1. Internal Scan Control Interface Signals

Signal	Type	Description	Clock
TestSE	I, CMOS, PD	Reserved for manufacturing test. Shall be tied to GND.	strap
TestMode	I, CMOS, PD	Reserved for manufacturing test. Shall be tied to GND.	strap
TestSignalIn[1:6]	I, CMOS	Reserved for manufacturing test. Shall be tied to GND.	strap
TestSignalOut[1:5]	O, CMOS, LD	Reserved for manufacturing test.	open

Table 6-2. Test Access Port interface signals

Signal	Type	Description	Clock
JtagTck	I, CMOS, PD	JTAG TAP Test Clock	-
JtagTdi	I, CMOS, PD	JTAG TAP Test Data In	*JtagTck*
JtagTms	I, CMOS, PD	JTAG TAP Test Mode Select	*JtagTck*
JtagTRstN	I, CMOS, PD	JTAG TAP Test Reset	*JtagTck*
JtagTdo	O, CMOS, LD	JTAG TAP Test Data Out	*JtagTck*

Table 6-3. Clocks and Reset interface signals

Signal	Type	Description	Clock
SysClk	I, CMOS	The main source clock. Can be configured to be the source clock for the *SpwClk* and *TmClk* as well.	-
SpwClk	I, CMOS	May be connected inside the AT7909E to the internal *SpwClk*	-
TmClk1	I, CMOS	May be connected inside the AT7909E to the *TmClk*	-
TmClk2	I, CMOS	May be connected inside the AT7909E to the *TmClk*	-
PoResetN	I, Schmitt	Power On Reset. (Full reset)	-

Table 6-4. Configuration interface signals

Signal	Type	Description	Clock
Irq	O, CMOS, LD	Interrupt	*SysClk*
ReInit	I, Schmitt, PD	Re-initialise.	-

6.2 Memory Interface

Signal	Type	Description	Clock
MemSize16	I, CMOS	Configuration for *PromCsN* area width	strap
MemD[15:0]	IO, CMOS, PD	Memory Data (big-endian)	*SysClk*
MemDcc[5:0]	IO, CMOS, PD	Memory Check Bits	*SysClk*
MemA[19:0]	O, CMOS, HD	Memory Address (byte address)	*SysClk*
MemOEN	O, CMOS, HD	Memory Output Enable	*SysClk*
MemWEN	O, CMOS, HD	Memory Write Enable	*SysClk*
PromCsN	O, CMOS, HD	Configuration PROM chip select	*SysClk*
ExtRecLacN	O, CMOS, HD	External Recovery LAC select (when external LAC is used)	*SysClk*
RamCsN	O, CMOS, HD	SRAM chip select	*SysClk*

6.3 Packet Telecommand Decoder Module (PDEC3) signals

Signal	Type	Description	Clock
PdecMapAdt	O, CMOS, LD	MAP Packet Abort.	*SysClk*
PdecMapClk	O, CMOS, MD	MAP Serial Clock.	*SysClk*
PdecMapData	O, CMOS, LD	MAP Serial Data.	*SysClk*
PdecMapDtrG	I, CMOS, PD	MAP data terminal ready. The asynchronous *PdecMapDtrG* input indicates that the destination for the general MAP interface is ready to receive the TC Segment, which can be used for flow control. When the input is high, the TC Segment will be transferred.	-
PdecMapDsrG	O, CMOS, LD	MAP data set ready. The *PdecMapDsrG* output indicates that a TC Segment is available for transfer on the general MAP interface. When the output is high the TC Segment is ready.	*SysClk*
PdecMapGenA[5:0]	O, CMOS, LD	6 bits MapGen address. These bits are generated from the real MAP address using the MAP allocation table.	*SysClk*
PdecMapDsr[1:5]	O, CMOS, LD	MAP data set ready. Each *PdecMapDsr** output indicates that a TC Segment is available for transfer on the corresponding MAP interface. When the output is high the TC Segment is ready. Only one *PdecMapDsr** output is active at any one time.	*SysClk*
PdecMapDtr[1:5]	I, CMOS, PD	MAP data terminal ready. Each asynchronous *PdecMapDtr** input indicates that the corresponding destination is ready to receive the TC Segment, which can be used for flow control. When the input is high, the TC Segment will be transferred.	-
PdecTcAct[5:0]	I, Schmitt, PD	TC channel active inputs, which serves as enable signals for the corresponding *PdecTcIn** and *PdecTcClk** inputs. A TC channel is active when its *PdecTcAct** input is high. These inputs can be asynchronous.	-
PdecTcClk[5:0]	I, Schmitt, PD	TC symbol clock inputs, recognised when the corresponding *PdecTcAct** input is asserted. These inputs can be asynchronous w.r.t. the clock.	-
PdecTcIn[5:0]	I, Schmitt, PD	TC symbol data stream inputs. The data shall be valid on the falling edge of the corresponding PdecTcClk* input.	-
PdecRfAvN[0:3]	I, Schmitt, PD	RF available indication for the CLCW. When the input is low, the "No RF Available" flag in the CLCW will be set to logic zero.	-

Signal	Type	Description	Clock
PdecClcwClk[0:1]	I, Schmitt, PD	CLCW clock. This asynchronous input clocks out the CLCW status using a protocol based on synchronous bit serial acquisition.	-
PdecClcwSamp[0:1]	I, Schmitt, PD	CLCW sample. This input sample the CLCW status before it is clocked out using a protocol based on synchronous bit serial acquisition. The CLCW is transferred when *PdecClcwSamp** is high. Each input must be synchronous to the corresponding *PdecClcwClk** input.	-
PdecClcwD[0:1]	O, CMOS, LD	CLCW data. This output provide the CLCW data serially after the rising edge of the corresponding *PdecClcwSamp** input or after the rising edge of the corresponding *PdecClcwClk** input.	*SysClk*
PdecMapSwitch	I, CMOS, PD	Swaps the signals between MAP interface 1 and MAP interface 2.	-
PdecTcPrior	I, CMOS, PD	TC channel priority mode configuration. When this static input is high, the active TC channels are selected with priority.	strap
PdecAuEnable	I, Schmitt, PD	AU enable input.	-

6.4 External CPDU Interfaces (ExtCpduIf) signals

Signal	Type	Description	Clock
ExtCpduIfClk	I, Schmitt, PD	Packet Wire serial bit clock	-
ExtCpduIfValid	I, Schmitt, PD	Packet valid	*ExtCpduIfClk*
ExtCpduIfRdy	O, CMOS, LD	Receiver ready, i.e. the interface is ready to receive a TC Segment.	*SysClk*
ExtCpduIfData	I, Schmitt, PD	Serial data	*ExtCpduIfClk*
ExtCpduIfAbort	I, Schmitt, PD	Abort packet	*ExtCpduIfClk*

6.5 CPDM Selector Module (CSEL) signals

Signal	Type	Description	Clock
CselStatusIn[2:0]	I, Schmitt, PD	Remote CSEL status	-
CselStatusOut[2:0]	O, CMOS, LD	CSEL status exchange	*SysClk*
CselRmOn	I, Schmitt, PD	Enables RM input access to the CPDM via the CSEL. When deasserted, it disables the RM input, i.e. if the ExtCpduIf is internally connected to the RM input it will not be able to transmit any pulse commands.	-

6.6 Command Pulse Distribution Module (CPDM) signals

Signal	Type	Description	Clock
CpdmStrb	O, CMOS, LD	This active high output provides the CPDU output pulse timing.	*SysClk*
CpdmArmN	O, CMOS, LD	This active low output provides an arming signal which can be used to power-on the CPDU output drivers	*SysClk*
CpdmSer	O, CMOS, MD	The pulse number is distributed serially.	*SysClk*
CpdmClk	O, CMOS, MD	Bit clock for the CpdmSer output	*SysClk*
CpdmClkAlive	I, Schmitt	Input indicating that the *CpdmClkToggle* is still toggling	-
CpdmClkToggle	O, CMOS, MD	The CPDM internal clock available as an external pin.	*SysClk*

6.7 Packet Telemetry Encoder Module (TME) signals

Signal	Type	Description	Clock
TmeClcwClk	O, CMOS, LD	CLCW clock. This output clocks out the CLCW status using a synchronous bit serial protocol.	*TmClk*
TmeClcwSamp	O, CMOS, LD	CLCW sample. This input defines the transfer of the CLCW using a synchronous bit serial protocol; the CLCW is transferred when *TmeClcwSamp* is set high.	*TmClk*
TmeClcwD[0:3]	I, CMOS, PD	Serial CLCW data. These inputs shall provide the data serially after the rising edge of the *TmeClcwSamp* input and after the rising edges of the *TmeClcwClk* input.	-
TmeUnEncClk	O, CMOS, HD	Clock output for the unencoded serial transfer frame, used to clock out *UnEncOut* and *UnEncSync*.	*TmClk*
TmeUnEncOut	O, CMOS, HD	Unencoded serial TM transfer frame output. This output is driven on the rising edge of *UnEncClk*.	*TmClk*
TmeUnEncSync	O, CMOS, MD	Synchronisation marker output indicator. This output is driven on the rising edge of *UnEncClk*, and it is set high while the synchronisation marker is output on *UnEncOut*.	*TmClk*
TmeEncClk	O, CMOS, HD	Clock output for the encoded serial transfer frames, used to clock out *TmeEncOut*.	*TmClk*
TmeEncOut	O, CMOS, HD	Encoded serial TM transfer frame output. This output is driven on the rising edge of *TmeEncClk*.	*TmClk*
TmeEncIQClk	O, CMOS, MD	Clock output for I/Q modulated output, used to clock out data on *TmeEncIOut* and *TmeEncQOut.*	*TmClk*
TmeEncIOut	O, CMOS, MD	I/Q modulated data output. This output is driven on the rising edge of *TmeEncIQClk*.	*TmClk*

Signal	Type	Description	Clock
TmeEncQOut	O, CMOS, MD	I/Q modulated data output. This output is driven on the rising edge of *TmeEncIQClk*.	*TmClk*
TmeTimeStrb	O, CMOS, LD	Time Sampling strobe output. Asserted to indicate that the on-board time should be sampled.	*TmClk*
TmeEnable	I, Schmitt, PD	Enable signal for the whole TME. When asserted the TME is enabled. When deasserted then all outputs from the TME are deasserted (inactive).	-
TmeSClk[A:H]	I, CMOS, PD	Packet Wire Serial Interface Clock. This input clocks serial data into a Virtual Channel serial interface.	-
TmeSIn[A:H]	I, CMOS, PD	Packet Wire Serial Data input. This input is sampled on the rising edge of TmeSClk* when TmeSValid is asserted.	-
TmeSRdy[A:H]	O, CMOS, LD	Packet Wire Virtual channel Ready. This signal is asserted to indicate that two octets can be received.	*SysClk*
TmeSValid[A:H]	I, CMOS, PD	Packet Wire Serial Interface Data Valid. This signal informs the corresponding VC interface when a telemetry packet begins/ends, and it also defines the byte boundaries in the input data stream. Input shall be asserted while data is being input.	-

6.8 SpaceWire Module (SPW) signals

Signal	Type	Description	Clock
SpwDInA	I, CMOS	SpaceWire Serial Data Input from link A	-
SpwSInA	I, CMOS	SpaceWire Serial Strobe Input from link A	-
SpwDInB	I, CMOS	SpaceWire Serial Data Input from link B	-
SpwSInB	I, CMOS	SpaceWire Serial Strobe Input from link B	-
SpwDOut	O, CMOS, MD	SpaceWire Serial Data Output	*SpwClk*
SpwSOut	O, CMOS, MD	SpaceWire Serial Strobe Output	*SpwClk*
SpwIfSel	I, Schmitt, PD	Used for switching between the two SpaceWire interfaces, Low =A and High = B.	-

6.9 Control Interface Module (CI) signals

Signal	Type	Description	Clock
CiInClk	I, CMOS, PD	Input Packet Wire Serial Clock	-
CiInData	I, CMOS, PD	Input Packet Wire Serial Data	*CiInClk*
CiInRdy	O, CMOS, MD	Input Packet Wire Receiver Ready	*SysClk*
CiInValid	I, CMOS, PD	Input Packet Wire Packet Valid	*CiInClk*
CiOutClk	O, CMOS, MD	Output Packet Wire Serial Clock	*SysClk*

CiOutData	O, CMOS, MD	Output Packet Wire Serial Data	*SysClk*
CiOutRdy	I, CMOS, PD	Output Packet Wire Receiver Ready	-
CiOutValid	O, CMOS, MD	Output Packet Wire Packet Valid	*SysClk*

7. Electrical characteristics

7.1 Absolute maximum ratings

Type	Value
Ambient temperature – military range	-55 to 125°C
Supply voltage, V_{DD}	-0.5 to 4.0 V
Input voltage range	-0.5 to 6.0 V
Input Current per power pin	±60 mA
Input Current per signal pin	±10 mA
Soldering Lead Temp. 1.6 mm from case for max 10 s	300 °C
Storage Temperature	-65 to 150°C
Junction temperature	175°C

7.2 Operating conditions

Parameter	Min	Typ	Max	Unit
Supply voltage	3.0	3.3	3.6	V
Operating temperature range	-55		125	°C

7.3 DC characteristics

Specified according to operating conditions table.

Parameter		Min	Typ	Max	Unit	Condition
V_{IH}	High level input voltage	2.0			V	CMOS and Schmitt
V_{IL}	Low level input voltage			0.8	V	CMOS and Schmitt
V_{HYS}	Hysteresis		0.61		V	Schmitt
V_{OH}	High level output voltage	2.4			V	
V_{OL}	Low level output voltage			0.4	V	
I_{IL}	Low level input current	-1		1	µA	Vin=GND, V_{DD}=V_{DD}(max)
I_{IH}	High level input current	-1		1	µA	Vin=V_{DD}=V_{DD}(max)
I_{IHP}	High level input current, pull-down input	5	30	70	µA	Vin=V_{DD}=V_{DD}(max)
I_{OZ}	Output leakage current	-1		1	µA	Outputs disabled, GND < Vout < VDD
I_{OZHP}	Output leakage current, pull-down output	5		70	µA	Outputs disabled, Vout = VDD
C_{IN}	Input pin capacitance			3	pF	
C_{IO}	I/O pin capacitance			7	pF	

7.4 Power consumption

Specified according to operating conditions table.

Parameter		Min	Max	Unit	Condition
I_{DDSBA}	Standby supply current for array		4.5	mA	Static mode
I_{DDOP}	Operating current for array		80	mA	VDD=3.6V

7.5 AC characteristics

Specified according to operating conditions table.
Following table gives the limit of the tested timings. The timing limits guaranteed by timing analysis based on MH1RT library, performed on SCTMTC Asic are given in 'SCTMTC User's Manual reference P-ASIC-NOT-00122-SE'.

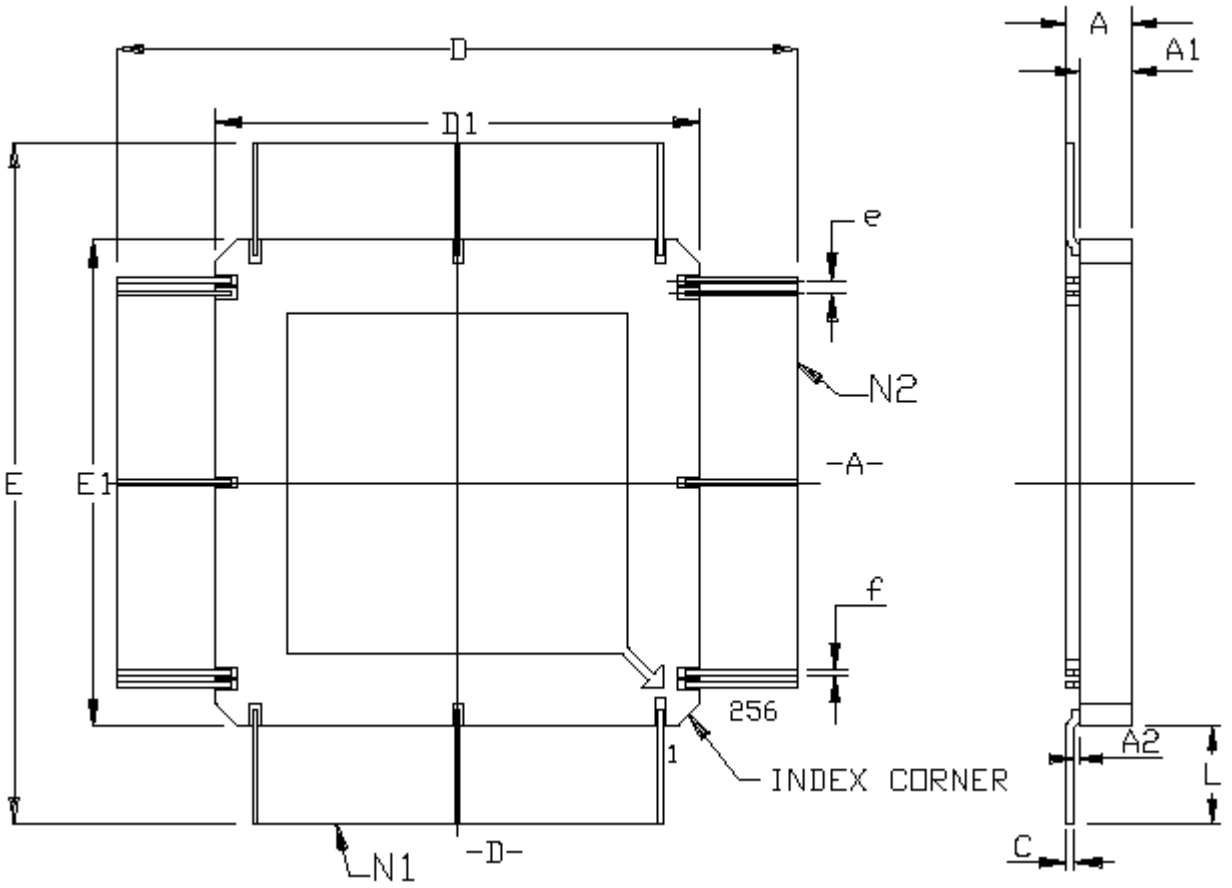
Parameter		Condition	Min	Max	Unit
Ts1	Setup time SpwIfSel to SysClk	VDD = 3.6 V note1		0	ns
Ts2	Setup time MemD[15:0] to SysClk MemDcc[5:0] to SysClk	VDD = 3.6 V note1		0	ns
Tp1	Propagation Delay SysClk to MemA[23:0]	VDD = 3.0 V note1		30	ns
Tp2	Propagation Delay SysClk to MemD[15:0] SysClk to MemDcc[5:0]	VDD = 3.0 V note1		42	ns
Tp3	Propagation Delay SysClk to SpwDOut	VDD = 3.0 V note1		41	ns
Tp4	Propagation Delay SysClk to SpwDOut	VDD = 3.0 V note1		34	ns
Tp5	Propagation Delay SysClk to SpwSOut	VDD = 3.0 V note1		41	ns
Tp6	Propagation Delay SysClk to SpwSOut	VDD = 3.0 V note1		34	ns
Tp7	Propagation Delay SysClk to SeqIrq	VDD = 3.0 V note1		53	ns

Note 1: Test conditions:
Tester load *80 pF*
VIL = 0V, VIH = VDD
Input signals dynamic characteristics: tr,tf < 10ns
Threshold voltages: VOL = VOH = VDD/2.

8. Functional description

8.1 Package

The package is a 256-pin MQFP with 0.02 mil pin spacing and lid connected to ground.



	mm		inch	
A	2.41	3.18	0.095	0.125
A1	2.06	2.56	0.081	0.101
A2	0.05	0.36	0.002	0.014
C	0.10	0.20	0.004	0.008
D/E	53.23	55.74	2.095	2.195
D1/E1	36.83	37.34	1.450	1.470
e	0.508 BSC		0.020 BSC	
f	0.15	0.25	0.006	0.010
L	8.20	9.20	0.323	0.362
N1	64			
N2	64			

9. Pins assignment

Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name
1	*Vss[8]*	53	*MemA[3]*	105	*SysClk*	157	*TmeSValid[D]*
2	*MemD[12]*	54	*MemA[2]*	106	*PoResetN*	158	*TmeSIn[D]*
3	*MemD[11]*	55	*Vss[1]*	107	*PdecTcIn[5]*	159	*TmeSClk[D]*
4	*MemD[10]*	56	*MemA[1]*	108	*PdecTcClk[5]*	160	*Vss[14]*
5	*Vdd[8]*	57	*Vss[19]*	109	*PdecTcAct[5]*	161	*TmeSRdy[C]*
6	*MemD[9]*	58	*Vdd[19]*	110	*PdecTcIn[4]*	162	*TmeSValid[C]*
7	*Vss[18]*	59	*MemA[0]*	111	*PdecTcClk[4]*	163	*TmeSIn[C]*
8	*Vdd[18]*	60	*Vdd[1]*	112	*PdecTcAct[4]*	164	*TmeSClk[C]*
9	*MemD[8]*	61	*MemSize16*	113	*PdecTcIn[3]*	165	*ExtCpduIfAbort*
10	*MemD[7]*	62	*TestSignalIn[1]*	114	*PdecTcClk[3]*	166	*TmeSValid[B]*
11	*MemD[6]*	63	*TestMode*	115	*PdecTcAct[3]*	167	*ExtCpduIfValid*
12	*MemD[5]*	64	*TestSE*	116	*PdecTcIn[2]*	168	*ExtCpduIfRdy*
13	*MemD[4]*	65	*JtagTdo*	117	*PdecTcClk[2]*	169	*ExtCpduIfData*
14	*MemD[3]*	66	*JtagTdi*	118	*Vss[15]*	170	*TmeSIn[B]*
15	*Vss[7]*	67	*JtagTms*	119	*PdecTcAct[2]*	171	*ExtCpduIfClk*
16	*TestSignalIn[6]*	68	*JtagTRstN*	120	*PdecTcIn[1]*	172	*TmeSClk[B]*
17	*MemD[2]*	69	*JtagTck*	121	*Vss[21]*	173	*TmeSRdy[B]*
18	*MemD[1]*	70	*PdecMapGenA[5]*	122	*Vdd[21]*	174	*TmeSRdy[A]*
19	*Vdd[7]*	71	*Vss[20]*	123	*PdecTcClk[1]*	175	*TmeSValid[A]*
20	*MemD[0]*	72	*Vdd[20]*	124	*Vdd[15]*	176	*TmeSIn[A]*
21	*MemCs3N*	73	*PdecMapGenA[4]*	125	*PdecTcAct[1]*	177	*TmeSClk[A]*
22	*Vss[6]*	74	*PdecMapGenA[3]*	126	*PdecTcIn[0]*	178	*TmeEnable*
23	*PdecTcPrior*	75	*PdecMapGenA[2]*	127	*PdecTcClk[0]*	179	*Vdd[14]*
24	*MemCs2N*	76	*PdecMapGenA[1]*	128	*PdecTcAct[0]*	180	*TmeTimeStrb*
25	*MemCs0N*	77	*PdecMapGenA[0]*	129	*PdecClcwD[1]*	181	*TmeUnEncSync*
26	*Vdd[6]*	78	*Vss[17]*	130	*PdecClcwSamp[1]*	182	*TmeUnEncClk*
27	*MemOEN*	79	*PdecMapDtr[5]*	131	*PdecClcwClk[1]*	183	*Vss[13]*
28	*MemWEN*	80	*PdecMapDsr[5]*	132	*PdecMapSwitch*	184	*TmeUnEncOut*
29	*Vss[5]*	81	*PdecMapDtr[4]*	133	*TmeSValid[H]*	185	*Vss[23]*
30	*MemA[19]*	82	*PdecMapDsr[4]*	134	*PdecAuEnable*	186	*Vdd[23]*
31	*MemA[18]*	83	*Vdd[17]*	135	*Vss[22]*	187	*Vdd[13]*
32	*Vdd[5]*	84	*PdecMapDtr[3]*	136	*Vdd[22]*	188	*TmeEncOut*
33	*MemA[17]*	85	*PdecMapDsr[3]*	137	*TmeSIn[H]*	189	*TmeEncClk*
34	*MemA[16]*	86	*PdecMapDtr[2]*	138	*TmeSClk[H]*	190	*TmeEncIOut*
35	*Vss[4]*	87	*PdecMapDsr[2]*	139	*TmeSRdy[H]*	191	*TmeEncQOut*
36	*MemA[15]*	88	*PdecMapDtr[1]*	140	*TmeSValid[G]*	192	*TmeEncIQClk*
37	*MemA[14]*	89	*PdecMapDsr[1]*	141	*TestSignalIn[4]*	193	*Vss[12]*
38	*Vdd[4]*	90	*PdecMapDtrG*	142	*TmeSIn[G]*	194	*TmeClcwSamp*
39	*MemA[13]*	91	*PdecMapDsrG*	143	*TmeSClk[G]*	195	*TmeClcwClk*

Pin	Signal name	Pin	Signal name	Pin	Signal name	Pin	Signal name
40	*MemA[12]*	92	*PdecMapData*	144	*TmeSRdy[G]*	196	*TmeClcwD[3]*
41	*MemA[11]*	93	*PdecMapClk*	145	*TmeSValid[F]*	197	*TmeClcwD[2]*
42	*Vss[3]*	94	*PdecRfAvN[3]*	146	*TmeSIn[F]*	198	*TmeClcwD[1]*
43	*MemA[10]*	95	*PdecRfAvN[2]*	147	*TmeSRdy[F]*	199	*Vss[24]*
44	*Vdd[3]*	96	*Vss[16]*	148	*TmeSClk[F]*	200	*Vdd[24]*
45	*MemA[9]*	97	*PdecMapAdt*	149	*TmeSValid[E]*	201	*TmeClcwD[0]*
46	*MemA[8]*	98	*PdecRfAvN[1]*	150	*PdecClcwD[0]*	202	*ReInit*
47	*MemA[7]*	99	*Vdd[16]*	151	*PdecClcwSamp[0]*	203	*CiInClk*
48	*Vss[2]*	100	*PdecRfAvN[0]*	152	*TmeSIn[E]*	204	*CiInData*
49	*MemA[6]*	101	*TestSignalIn[2]*	153	*PdecClcwClk[0]*	205	*Vdd[12]*
50	*MemA[5]*	102	*TestSignalIn[3]*	154	*TmeSClk[E]*	206	*CiInRdy*
51	*Vdd[2]*	103	*TmClk1*	155	*TmeSRdy[E]*	207	*CiInValid*
52	*MemA[4]*	104	*TmClk2*	156	*TmeSRdy[D]*	208	*CiOutRdy*
209	*CiOutClk*	222	*SpwDOut*	235	*Irq*	248	*MemDcc[3]*
210	*CiOutData*	223	*CpdmClkAlive*	236	*CselStatusOut[2]*	249	*Vss[25]*
211	*Vss[11]*	224	*CpdmClkToggle*	237	*CselStatusOut[1]*	250	*Vdd[25]*
212	*CiOutValid*	225	*CpdmClk*	238	*CselStatusOut[0]*	251	*MemDcc[2]*
213	*TestSignalOut[1]*	226	*Vss[10]*	239	*TestSignalOut[2]*	252	*MemDcc[1]*
214	*SpwSInB*	227	*CpdmSer*	240	*TestSignalOut[3]*	253	*MemDcc[0]*
215	*SpwDInB*	228	*CpdmArmN*	241	*Vss[9]*	254	*MemD[15]*
216	*SpwIfSel*	229	*CpdmStrb*	242	*TestSignalOut[4]*	255	*MemD[14]*
217	*SpwSInA*	230	*CselRmOn*	243	*TestSignalOut[5]*	256	*MemD[13]*
218	*SpwDInA*	231	*CselStatusIn[2]*	244	*TestSignalIn[5]*		
219	*SpwClk*	232	*CselStatusIn[1]*	245	*MemDcc[5]*		
220	*Vdd[11]*	233	*CselStatusIn[0]*	246	*MemDcc[4]*		
221	*SpwSOut*	234	*Vdd[10]*	247	*Vdd[9]*		

10. Ordering Information

Part number	Temperature range	Quality flow
AT7909EKA-E	25°C	Engineering sample
AT7909EKA-MQ	-55°C to +125°C	Mil Level B (*)
AT7909EKA-SV	-55°C to +125°C	Space Level B (*)

(*) according to Atmel Quality flow document reference 4288.

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