SINGLE 9-A HIGH SPEED LOW- SIDE MOSFET DRIVER WITH ENABLE

Check for Samples: UCC27321 , UCC27322, UCC37321, UCC37322

FEATURES

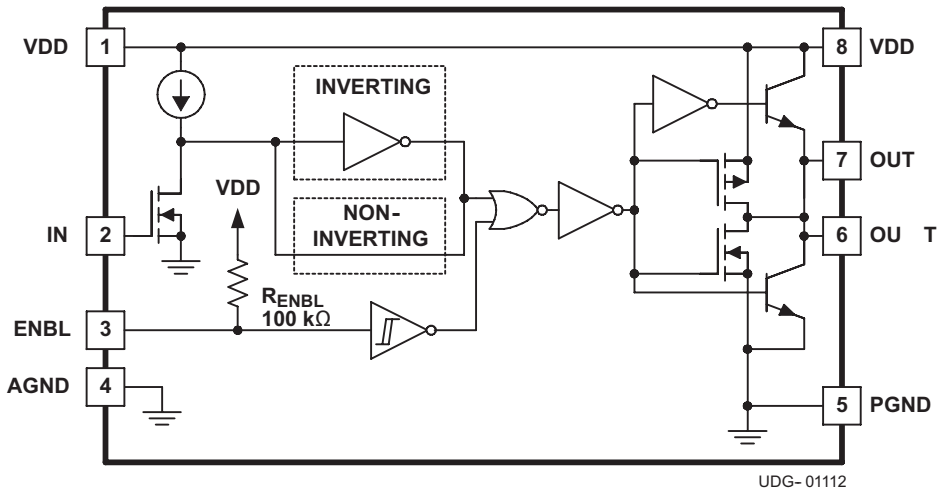
- Industry-Standard Pin-Out With Addition of Enable Funtion
- High-Peak Current Drive Capability of ±9 A at the Miller Plateau Region Using TrueDrive
- Efficient Constant Current Sourcing Using a Unique BiPolar & CMOS Output Stage
- TTL/CMOS Compatible Inputs Independent of Supply Voltage
- 20-ns Typical Rise and Fall Times with 10-nF Load
- Typical Propagation Delay Times of 25 ns With Input Falling and 35 ns with Input Rising
- 4-V to 15-V Supply Voltage
- Available in Thermally Enhanced MSOP PowerPAD™ Package With 4.7℃/W θjc
- Rated From –40℃ to 105℃
- Pb-Free Finish (NiPdAu) on SOIC-8 and PDIP-8 Packages

APPLICATIONS

- Switch Mode Power Supplies
- DC/DC Converters
- Motor Controllers
- Class-D Switching Amplifiers
- Line Drivers
- Pulse Transformer Driver

DESCRIPTION

The UCC37321/2 family of high-speed drivers deliver 9 A of peak drive current in an industry standard pinout. These drivers can drive the largest of MOSFETs for systems requiring extreme Miller current due to high dV/dt transitions. This eliminates additional external circuits and can replace multiple components to reduce space, design complexity and assembly cost. Two standard logic options are offered, inverting (UCC37321) and noninverting (UCC37322).



INPUT/OUTPUT TABLE

	ENBL	IN	OUT
INVERTING UCC37321	0	0	0
	0	1	0
	1	0	1
	1	1	0
NON-INVERTING UCC37322	0	0	0
	0	1	0
	1	0	0
	1	1	1

DESCRIPTION (CONTINUED)

Using a design that inherently minimizes shoot-through current, the outputs of these can provide high gate drive current where it is most needed at the Miller plateau region during the MOSFET switching transition. A unique hybrid output stage paralleling bipolar and MOSFET transistors (TrueDrive) allows efficient current delivery at low supply voltages.With this drive architecture, UCC37321/2/3 can be used in industry standard 6-A, 9-A and many 12-A driver applications. Latch up and ESD protection circuitries are also included. Finally, the UCC37321/2 provides an enable (ENBL) function to have better control of the operation of the driver applications. ENBL is implemented on pin 3 which was previously left unused in the industry standard pin-out. It is internally pulled up to Vdd for active high logic and can be left open for standard operation.

In addition to SOIC-8 (D) and PDIP-8 (P) package offerings, the UCC37321/2 also comes in the thermally enhanced but tiny 8-pin MSOP PowerPAD™ (DGN) package. The PowerPAD™ package drastically lowers the thermal resistance to extend the temperature operation range and improve the long-term reliability.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)(2)

		UCCx732x	UNIT
Supply voltage, V_{DD}		-–0.3 to 16	V
Output current (OUT) DC, I_{OUT_DC}		0.6	A
Input voltage (IN), V_{IN}		–0.3 V to 6 V or V_{DD}+0.3 (whichever is larger)	V
Enable voltage (ENBL)		–0.3 V to 6 V or V_{DD}+0.3 (whichever is larger)	
Power dissipation at T_A = 25℃	D package	650	mW
	DGN package	3	W
	P package	350	mW
Junction operating temperature, T_J		–55 to 150	℃
Storage temperature, T_{stg}		–65 to 150	℃
Lead temperature (soldering, 10 sec.)		300	℃

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

ORDERING INFORMATION

OUTPUT CONFIGURATION	TEMPERATURE RANGE $T_A = T_J$	PACKAGED DEVICES		
		SOIC-8 (D)(1)	MSOP-8 PowerPAD (DGN)(1)	PDIP-8 (P)
Inverting	–40℃ to +105℃	UCC27321D	UCC27321DGN	UCC27321P
	0℃ to +70℃	UCC37321D	UCC37321DGN	UCC37321P
NonInverting	–40℃ to +105℃	UCC27322D	UCC27322DGN	UCC27322P
	0℃ to +70℃	UCC37322D	UCC37322DGN	UCC37322P

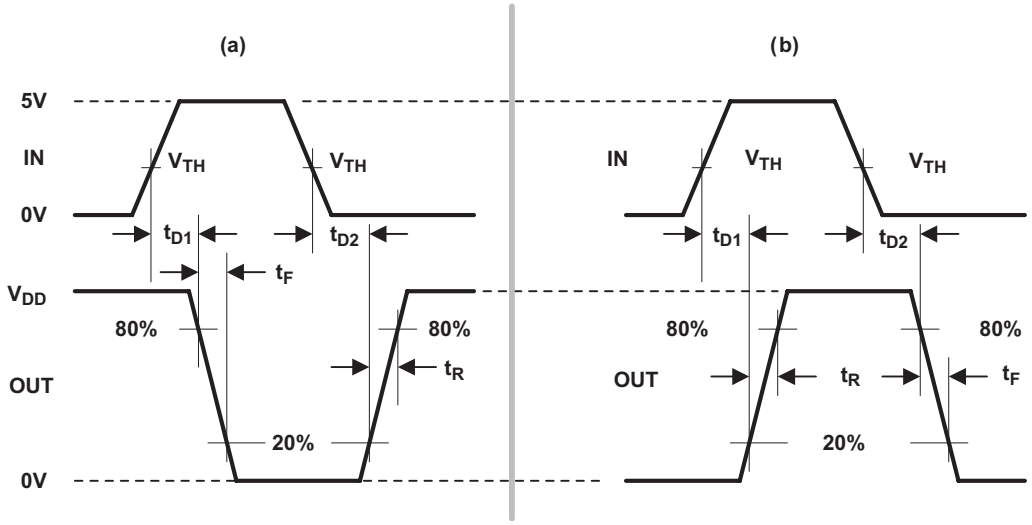
(1) D (SOIC–8) and DGN (PowerPAD–MSOP) packages are available taped and reeled. Add R suffix to device type (e.g. UCC37321DR, UCC37322DGNR) to order quantities of 2,500 devices per reel.

ELECTRICAL CHARACTERISTICS

V_{DD} = 4.5 V to 15 V, T_A = –40℃ to 105℃ for UCC2732x, T_A = 0℃ to 70℃ for UCC3732x, $T_A = T_J$, (unless otherwise noted)

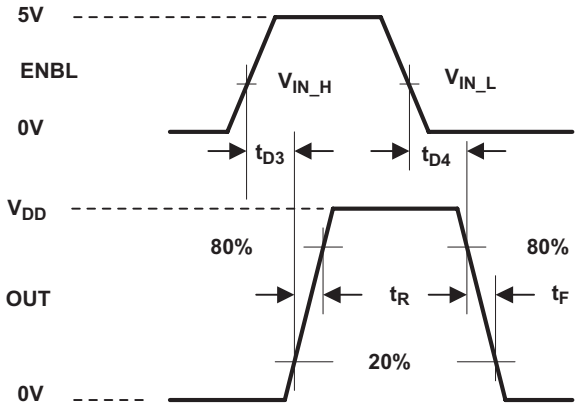
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input (IN)							
V_{IN_H}, logic 1 input threshold				2			V
V_{IN_H}, logic 1 input threshold						1	V
Input current		0 V ≤ V_{IN} ≤ V_{DD}		–10	0	10	µA
Output (OUT)							
Peak output current(1)(2)		V_{DD} = 14 V,			9		A
V_{OH}, output high level		$V_{OH} = V_{DD} – V_{OUT}$,	I_{OUT} = –10mA		150	300	mV
V_{OL}, output high level		I_{OUT} = 10 mA			11	25	mV
Output resistance high(3)		I_{OUT} = –10mA,	V_{DD} = 14 V		15	25	Ω
Output resistance low(3)		I_{OUT} = 10 mA, V	V_{DD} = 14		1.1	2.2	Ω
Latch--up protection(1)				500			mA
Overall							
I_{DD}, static operating current	UCC37321 UCC27321	IN = LO, EN = LO,	V_{DD} = 15 V		150	225	µA
		IN = HI, EN = LO,	V_{DD} = 15 V		440	650	
		IN = LO, EN = HI,	V_{DD} = 15 V		370	550	
		IN = HI, EN = HI,	V_{DD} = 15 V		370	550	
	UCC37322 UCC27322	IN = LO, EN = LO,	V_{DD} = 15 V		150	225	
		IN = HI, EN = LO,	V_{DD} = 15 V		450	650	
		IN = LO, EN = HI,	V_{DD} = 15 V		75	125	
		IN = HI, EN = HI,	V_{DD} = 15 V		675	1000	
Enable (ENBL)							
V_{IN_H}, high-level input voltage		LO to HI transition		1.7	2.2	2.7	V
V_{IN_L}, low-level input voltage		HI to LO transition		1.1	1.6	2.0	V
Hysteresis				0.25	0.55	0.90	
R_{ENBL}, enable impedance		V_{DD} = 14 V,	ENBL = GND	75	100	135	kΩ
t_{D3}, propagation delay time(4)		C_{LOAD} = 10 nF			60	90	ns
t_{D4}, propagation delay time(4)		C_{LOAD} = 10 nF			60	90	
Switching Time(5)							
t_R, rise time (OUT)		C_{LOAD} = 10 nF			20	70	ns
t_F, fall time (OUT)		C_{LOAD} = 10 nF			20	30	
t_{D1}, propagation delay, IN rising (IN to OUT)		C_{LOAD} = 10 nF			25	70	
t_{D2}, propagation delay, IN falling (IN to OUT)		C_{LOAD} = 10 nF			35	70	

(1) Ensured by design. Not tested in production.
(2) The pullup / pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors.
(3) The pullup / pulldown circuits of the driver are bipolar and MOSFET transistors in parallel. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor.
(4) See Figure 2.
(5) See Figure 1 for switching waveforms.



A. The 20% and 80% thresholds depict the dynamics of the BiPolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

Figure 1. Switching Waveforms for (a) Inverting Input to (b) Output Times

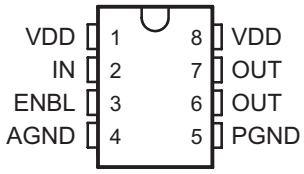


A. The 20% and 80% thresholds depict the dynamics of the BiPolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

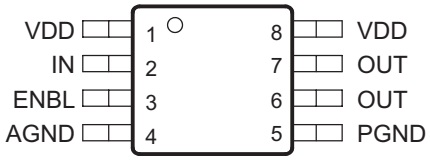
Figure 2. Switching Waveform for Enable to Output

PIN CONFIGURATIONS

PDIP (P) PACKAGE
(TOP VIEW)



SOIC (D) OR MSOP (DGN) PACKAGE
(TOP VIEW)



POWER DISSIPATION RATING TABLE

PACKAGE	SUFFIX	θjc (℃/W)	θja (℃/W)	Power Rating (mW) T_A = 70℃ (1)	Derating Factor Above 70℃ (mW/℃) (1)
SOIC-8	D	42	84 – 160 (2)	344 – 655 (2)	6.25 – 11.9 (2)
PDIP-8	P	49	110	500	9
MSOP PowerPAD-8	DGN	4.7	50 – 59	1370	17.1

(1) 125℃ operating junction temperature is used for power rating calculations
(2) The range of values indicates the effect of pc-board. These values are intended to give the system designer an indication of the best and worst case conditions. In general, the system designer should attempt to use larger traces on the pc-board where possible in order to spread the heat away form the device more effectively. For additional information on device temperature management, please refer to Packaging Information section of the *Power Supply Control Products Data Book*, (Ti Literature Number SLUD003).

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
AGND	4	–	The AGND and the PGND should be connected by a single thick trace directly under the device. There should be a low ESR, low ESL capacitor of 0.1 µF between VDD (pin 8) and PGND and a seperate 0.1-µF capacitor between VDD (pin 1) and AGND. The power MOSFETs should be located on the PGND side of the device while the control circuit should be on the AGND side of the device. The control circuit ground should be common with the AGND while the PGND should be common with the source of the power FETs.
ENBL	3	I	Enable input for the driver with logic compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to V_{DD} with 100-kΩ resistor for active high operation. The output state when the device is disabled will be low regardless of the input state.
IN	2	I	Input signal of the driver which has logic compatible threshold and hysteresis.
OUT	6, 7	O	Driver outputs that must be connected together externally. The output stage is capable of providing 9-A peak drive current to the gate of a power MOSFET.
PGND	5	–	Common ground for output stage. This ground should be connected very closely to the source of the power MOSFET which the driver is driving. Grounds are separated to minimize ringing affects due to output switching di/dt which can affect the input threshold.
VDD	1, 8	I	Supply voltage and the power input connections for this device. Three pins must be connected together externally.

APPLICATION INFORMATION

General Information

The UCC37321 and UCC37322 drivers serve as an interface between low-power controllers and power MOSFETs. They can also be used as an interface between DSPs and power MOSFETs. High-frequency power supplies often require high-speed, high-current drivers such as the UCC37321/2 family. A leading application is the need to provide a high power buffer stage between the PWM output of the control device and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the device drives the power device gates through a drive transformer. Synchronous rectification supplies also have the need to simultaneously drive multiple devices which can present an extremely large load to the control circuitry.

The inverting driver (UCC37321) is useful for generating inverted gate drive signals from controllers that have only outputs of the opposite polarity. For example, this driver can provide a gate signal for ground referenced, N-channel synchronous rectifier MOSFETs in buck derived converters. This driver can also be used for generating a gate drive signal for a P-channel MOSFET from a controller that is designed for N-channel applications.

MOSFET gate drivers are generally used when it is not feasible to have the primary PWM regulator device directly drive the switching devices for one or more reasons. The PWM device may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases theremay be a desire to minimize the effect of high frequency switching noise by placing the high current driver physically close to the load. Also, newer devices that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high impedance input to a driver such as the UCC37321/2. Finally, the control device may be under thermal stress due to power dissipation, and an external driver can help by moving the heat from the controller to an external package.

Input Stage

The IN threshold has a 3.3-V logic sensitivity over the full range of VDD voltages; yet, it is equally compatible with 0 V toVDD signals. The inputs of UCC37321/2 family of drivers are designed to withstand 500-mA reverse current without either damage to the device or logic upset. In addition, the input threshold turn-off of the UCC37321/2 has been slightly raised for improved noise immunity. The input stage of each driver should be driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns). The IN input of the driver functions as a digital gate, and it is not intended for applications where a slow changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limiting the rise or fall times to the power device is desired, then an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor may also help remove power dissipation from the device package, as discussed in the section on Thermal Considerations.

Output Stage

The TrueDrive output stage is capable of supplying ±9-A peak current pulses and swings to both VDD and GND and can encourage even themost stubborn MOSFETs to switch. The pull-up/pull-down circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the internal MOSFET. This means that in many cases, external-schottky-clamp diodes are not required.

This unique BiPolar and MOSFET hybrid output architecture (TrueDrive) allows efficient current sourcing at low supply voltages. The UCC37321/2 family delivers 9 A of gate drive where it is most needed during the MOSFET switching transition – at the Miller plateau region – providing improved efficiency gains.

Source/Sink Capabilities during Miller Plateau

Large power MOSFETs present a significant load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC37321/2 drivers have been optimized to provide maximum drive to a power MOSFET during the Miller Plateau Region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver device. [1]

Two circuits are used to test the current capabilities of the UCC37321/2 driver. In each case external circuitry is added to clamp the output near 5 V while the device is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test there is a transient period where the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient.

The circuit in Figure 3 is used to verify the current sink capability when the output of the driver is clamped around 5 V, a typical value of gate-source voltage during the Miller Plateau Region. The UCC37321 is found to sink 9 A at V_{DD} = 15 V.

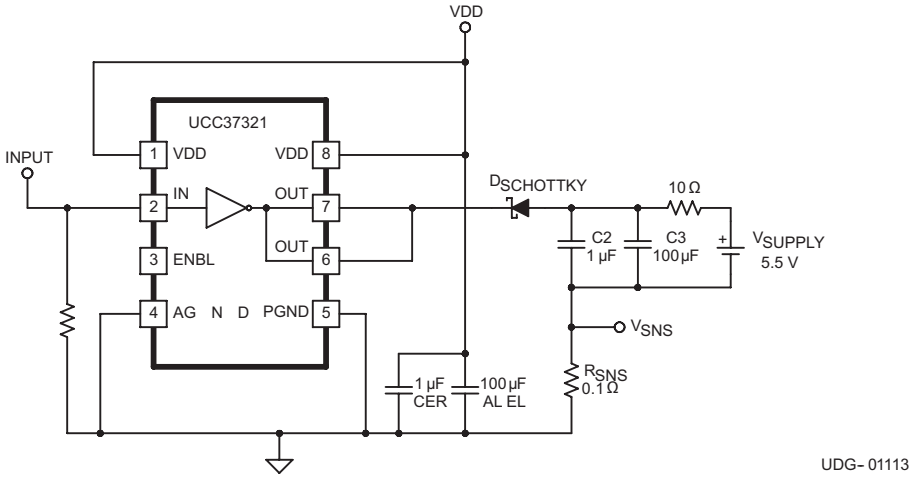


Figure 3. Sink Current Test Circuit

The circuit in Figure 4 is utilized to test the current source capability with the output clamped to around 5 V with a string of Zener diodes. The UCC37321 is found to source 9 A at V_{DD} = 15 V.

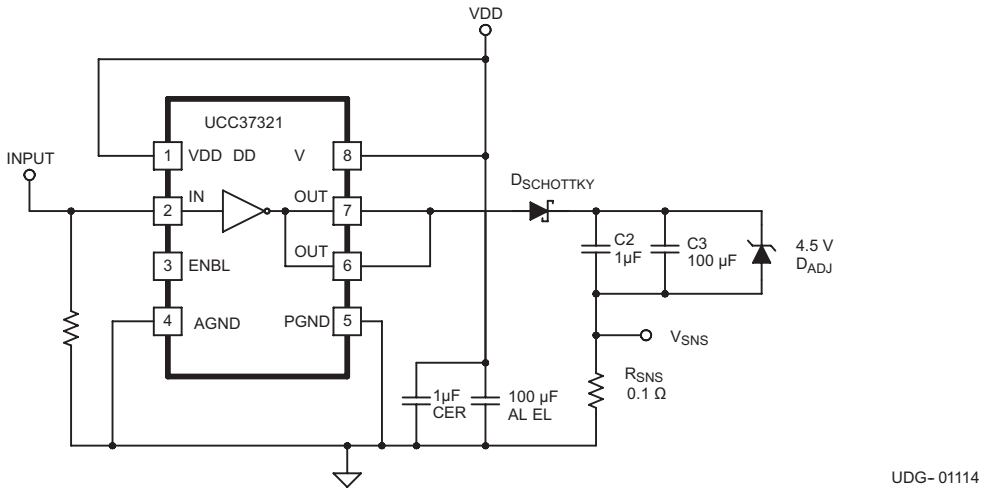


Figure 4. Source Current Test Circuit

It should be noted that the current sink capability is slightly stronger than the current source capability at lower VDD. This is due to the differences in the structure of the bipolar-MOSFET power output section, where the current source is a P-channel MOSFET and the current sink has an N-channel MOSFET.

In a large majority of applications it is advantageous that the turn-off capability of a driver is stronger than the turn-on capability. This helps to ensure that the MOSFET is held OFF during common power supply transients which may turn the device back ON.

Operational Circuit Layout

It can be a significant challenge to avoid the overshoot/undershoot and ringing issues that can arise from circuit layout.The low impedance of these drivers and their high di/dt can induce ringing between parasitic inductances and capacitances in the circuit. Utmost care must be used in the circuit layout.

In general, position the driver physically as close to its load as possible. Place a 1-µF bypass capacitor as close to the output side of the driver as possible, connecting it to pins 1 and 8. Connect a single trace between the two VDD pins (pin 1 and pin 8); connect a single trace between PGND and AGND (pin 5 and pin 4). If a ground plane is used, it may be connected to AGND; do not extend the plane beneath the output side of the package (pins 5 – 8). Connect the load to both OUT pins (pins 7 and 6) with a single trace on the adjacent layer to the component layer; route the return current path for the output on the component side, directly over the output path.

Extreme conditions may require decoupling the input power and ground connections from the output power and ground connections. The UCCx7321/2 has a feature that allows the user to take these extreme measures, if necessary. There is a small amount of internal impedance of about 15 Ω between the AGND and PGND pins; there is also a small amount of impedance (~30 Ω) between the two VDD pins. In order to take advantage of this feature, connect a 1-µF bypass capacitor between VDD and PGND (pins 5 and 8) and connect a 0.1-µF bypass capacitor between VDD and AGND (pins 1 and 4). Further decoupling can be achieved by connecting between the two VDD pins with a jumper that passes through a 40-MHz ferrite bead and connect bias power only to pin 8. Even more decoupling can be achieved by connecting between AGND and PGND with a pair of anti-parallel diodes (anode connected to cathode and cathode connected to anode).

VDD

Although quiescent VDD current is very low, total supply current will be higher, depending on OUTA and OUTB current and the operating frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from:

I_{OUT} = Qg x f, where f is frequency

For the best high-speed circuit performance, two V_{DD} bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-µF ceramic capacitor should be located closest to the VDD to ground connection. In addition, a larger capacitor (such as 1-µF) with relatively low ESR should be connected in parallel, to help deliver the high current peaks to the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels in the driver application.

Drive Current and Power Requirements

The UCC37321/2 family of drivers are capable of delivering 9-A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn an N-channel device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. An N-channel MOSFET is used in this discussion because it is the most common type of switching device used in high frequency power conversion equipment.

References 1 and 2 contain detailed discussions of the drive current required to drive a power MOSFET and other capacitive-input switching devices. Much information is provided in tabular form to give a range of the current required for various devices at various frequencies. The information pertinent to calculating gate drive current requirements will be summarized here; the original document is available from the TI website.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$E = \frac{1}{2}CV^2$, where C is the load capacitor and V is the bias voltage feeding the driver.

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by the following:

$P = 2 \times \frac{1}{2}CV^2f$, where f is the switching frequency.

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as:

$P = 10\ nF \times (12)^2 \times (300\ kHz) = 0.432\ W$

With a 12-V supply, this would equate to a current of:

$I = \frac{P}{V} = \frac{0.432\ W}{12\ V} = 0.036A$

The switching load presented by a power MOSFETcan be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence Qg = CeffV to provide the following equation for power:

$$P = C \times V^2 \times f = Qg \times V \times f$$

This equation allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

Enable

UCC37321/2 provides an Enable input for improved control of the driver operation. This input also incorporates logic compatible thresholds with hysteresis. It is internally pulled up to VDD with 100-kΩ resistor for active high operation. When ENBL is high, the device is enabled and when ENBL is low, the device is disabled. The default state of the ENBL pin is to enable the device and therefore can be left open for standard operation. The output state when the device is disabled is low regardless of the input state. See the truth table below for the operation using enable logic.

ENBL input is compatible with both logic signals and slow changing analog signals. It can be directly driven or a power-up delay can be programmed with a capacitor between ENBL and AGND.

Table 1. Input/Output Table

	ENBL	IN	OUT
INVERTING UCC37321	0	0	0
	0	1	0
	1	0	1
	1	1	0
NON-- INVERTING UCC37322	0	0	0
	0	1	0
	1	0	0
	1	1	1

THERMAL INFORMATION

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a power driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC37321/2 family of drivers is available in three different packages to cover a range of application requirements.

As shown in the power dissipation rating table, the SOIC-8 (D) and PDIP-8 (P) packages each have a power rating of around 0.5 W with T_A = 70℃. This limit is imposed in conjunction with the power derating factor also given in the table. Note that the power dissipation in our earlier example is 0.432W with a 10-nF load, 12 VDD, switched at 300 kHz. Thus, only one load of this size could be driven using the D or P package. The difficulties with heat removal limit the drive available in the D or P packages.

The MSOP PowerPAD-8 (DGN) package significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As illustrated in Reference 3, the PowerPAD packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board directly underneath the device package, reducing the θjc down to 4.7℃/W. Data is presented in Reference 3 to show that the power dissipation can be quadrupled in the PowerPAD configuration when compared to the standard packages. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference 4. This allows a significant improvement in heatsinking over that available in theDor P packages, and is shown to more than double the power capability of the D and P packages.

Note that the PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device.

References.

1. SEM-1400, Topic 2, *A Design and Application Guide for High Speed Power MOSFET Gate Drive Circuits*, TI Literature No. SLUP133
2. U-137, *Practical Considerations in High PerformanceMOSFET, IGBT andMCTGateDrive Circuits*, by Bill Andreycak, TI Literature No. SLUA105
3. Technical Brief, *PowerPad Thermally Enhanced Package*, TI Literature No. SLMA002
4. Application Brief, *PowerPAD Made Easy*, TI Literature No. SLMA004

Related Products

PRODUCT	DESCRIPTION	PACKAGES
UCC37323/4/5	Dual 4-A Low-Side Drivers	MSOP–8 PowerPAD, SOIC–8, PDIP–8
UCC27423/4/5	Dual 4-A Low-Side Drivers with Enable	MSOP–8 PowerPAD, SOIC–8, PDIP–8
TPS2811/12/13	Dual 2-A Low-Side Drivers with Internal Regulator	TSSOP–8, SOIC–8, PDIP–8
TPS2814/15	Dual 2-A Low-Side Drivers with Two Inputs per Channel	TSSOP–8, SOIC–8, PDIP–8
TPS2816/17/18/19	Single 2-A Low-Side Driver with Internal Regulator	5-Pin SOT–23
TPS2828/29	Single 2-A Low-Side Driver	5-Pin SOT–23

TYPICAL CHARACTERICTICS

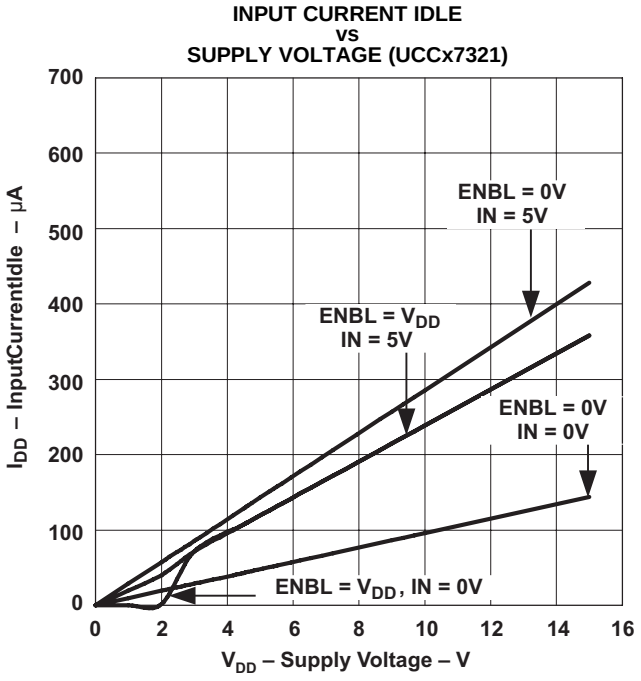


Figure 5.

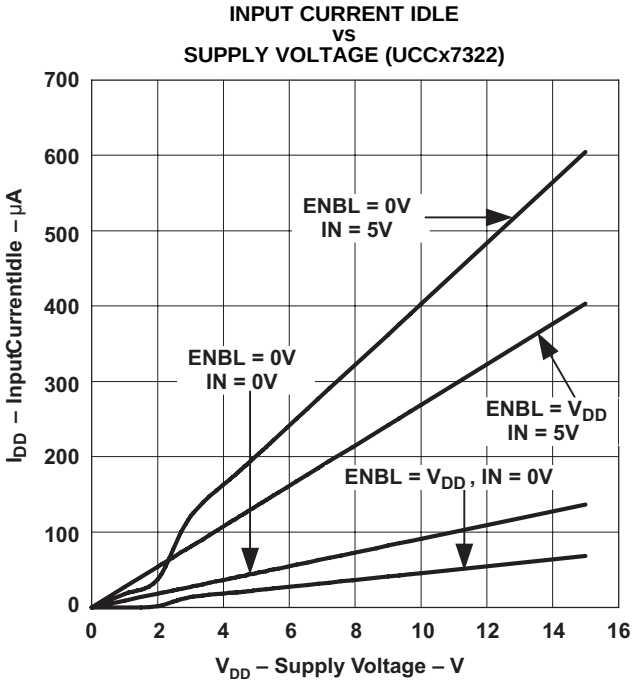


Figure 6.

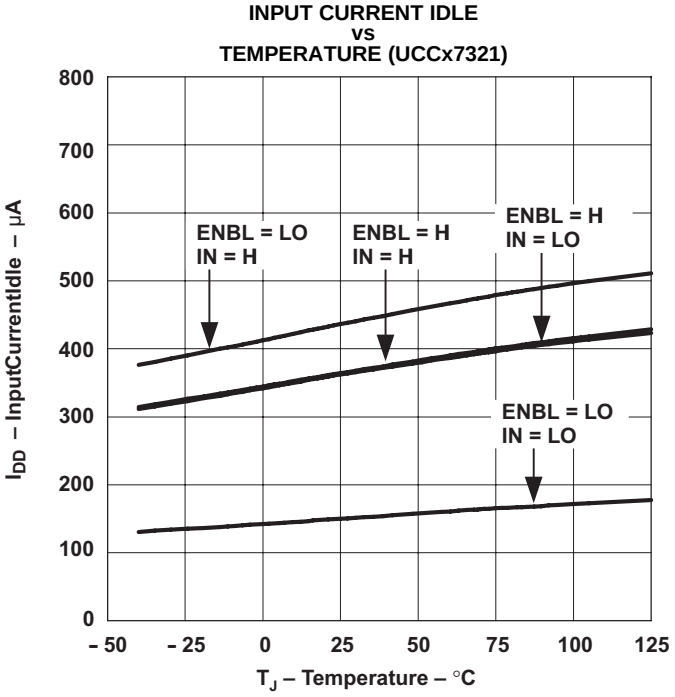


Figure 7.

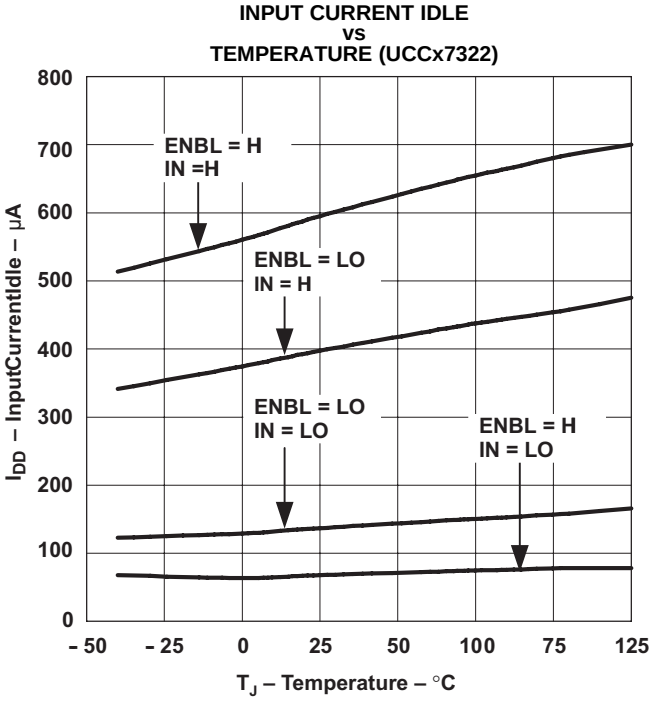


Figure 8.

TYPICAL CHARACTERICTICS (continued)

RISE TIME
vs
SUPPLY VOLTAGE

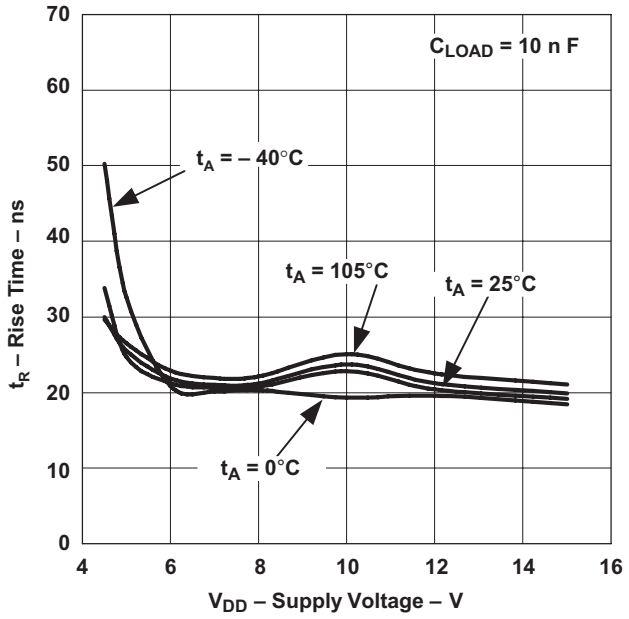


Figure 9.

FALL TIME
vs
SUPPLY VOLTAGE

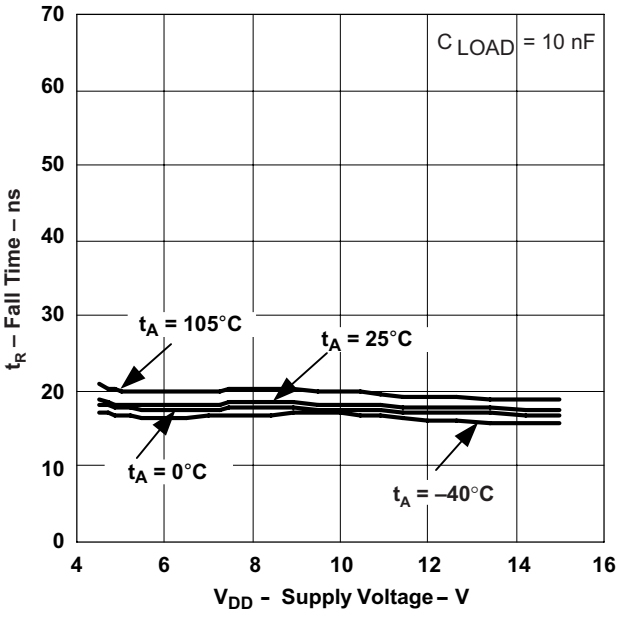


Figure 10.

RISE TIME
vs
LOAD CAPACITANCE

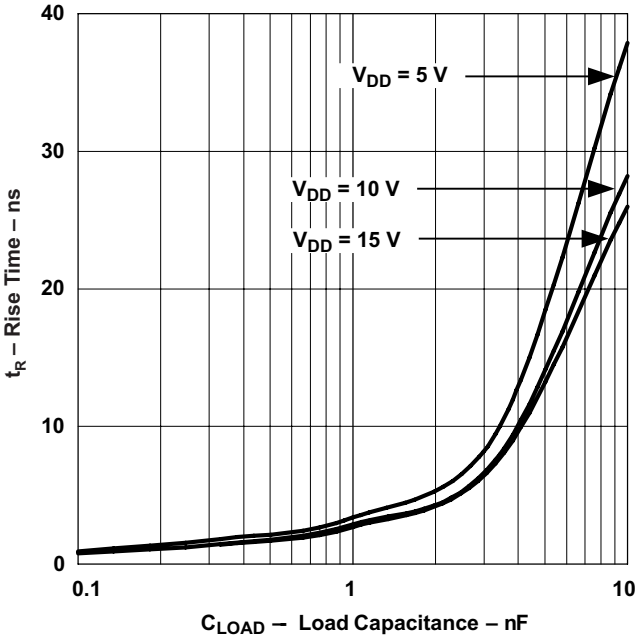


Figure 11.

FALL TIME
vs
OUTPUT CAPACITANCE

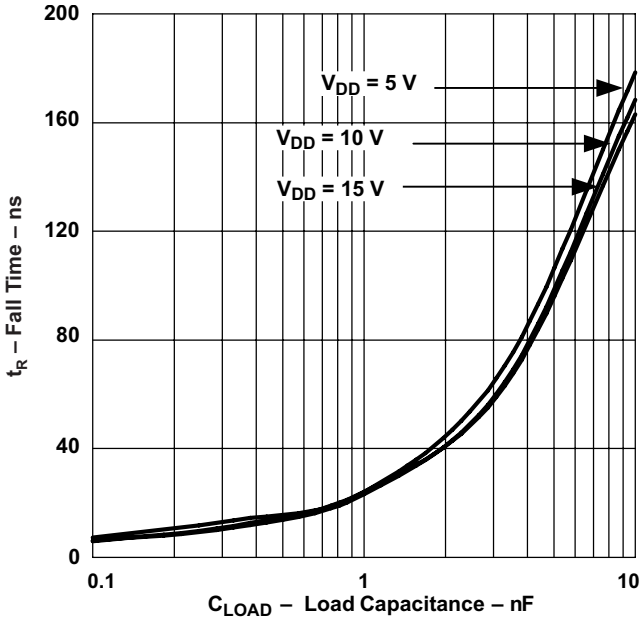


Figure 12.

TYPICAL CHARACTERICTICS (continued)

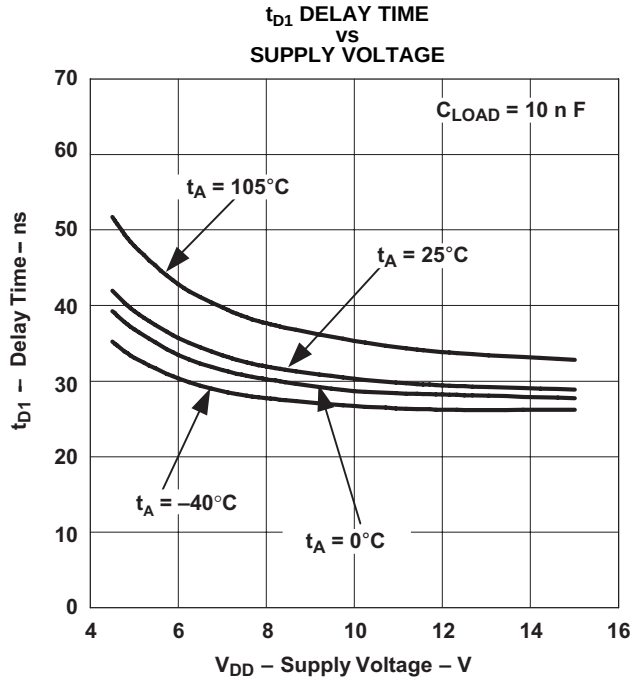


Figure 13.

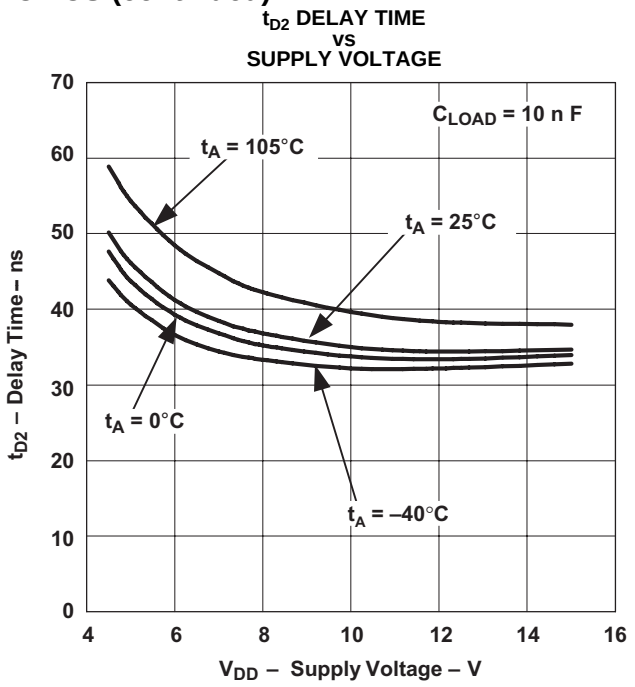


Figure 14.

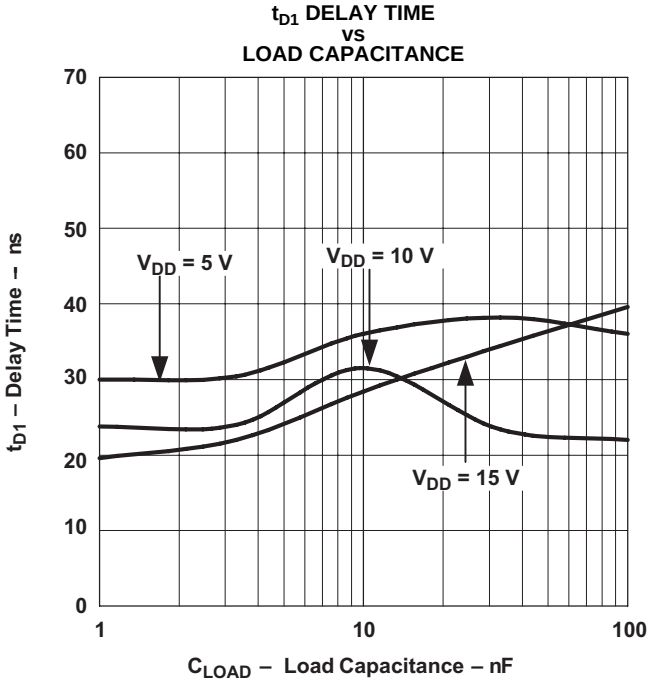


Figure 15.

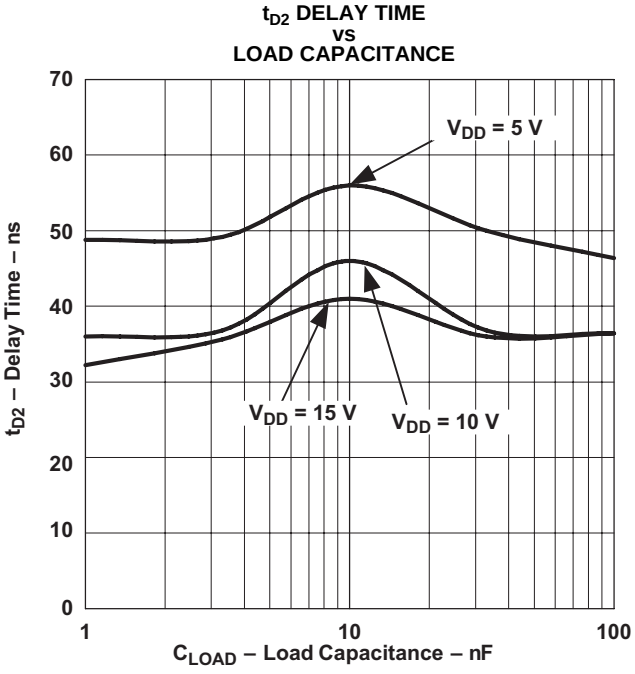


Figure 16.

TYPICAL CHARACTERICTICS (continued)

PROPAGATION TIMES
vs
PEAK INPUT VOLTAGE

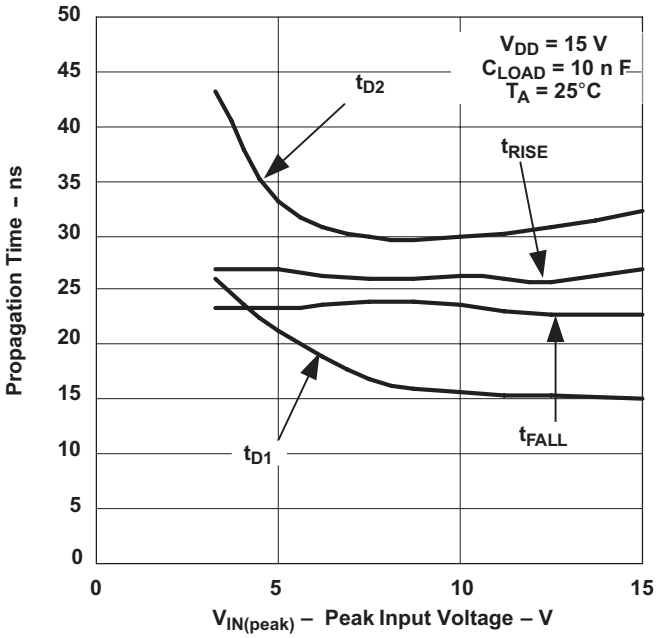


Figure 17.

INPUT THRESHOLD
vs
TEMPERATURE

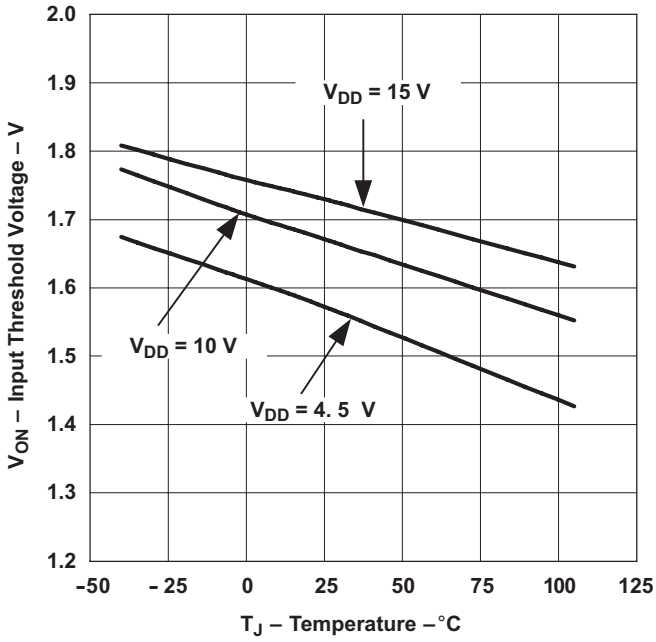


Figure 18.

ENABLE THRESHOLD AND HYSTERESIS
vs
TEMPERATURE

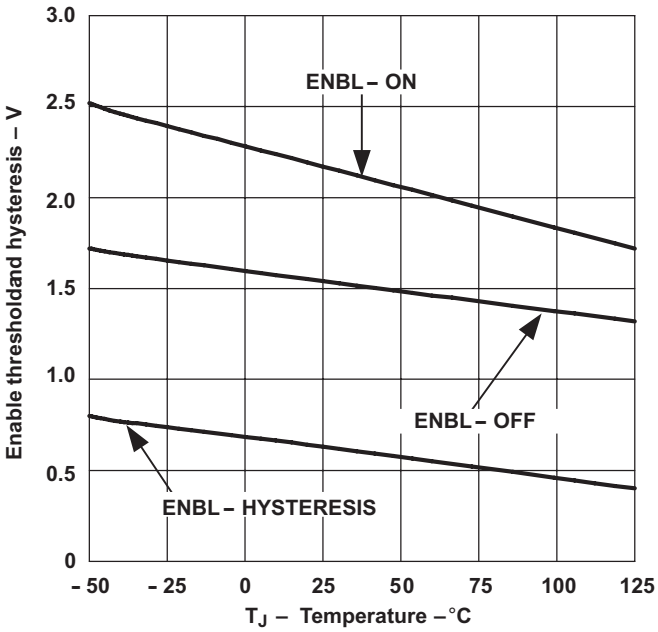


Figure 19.

ENABLE RESISTANCE
vs
TEMPERATURE

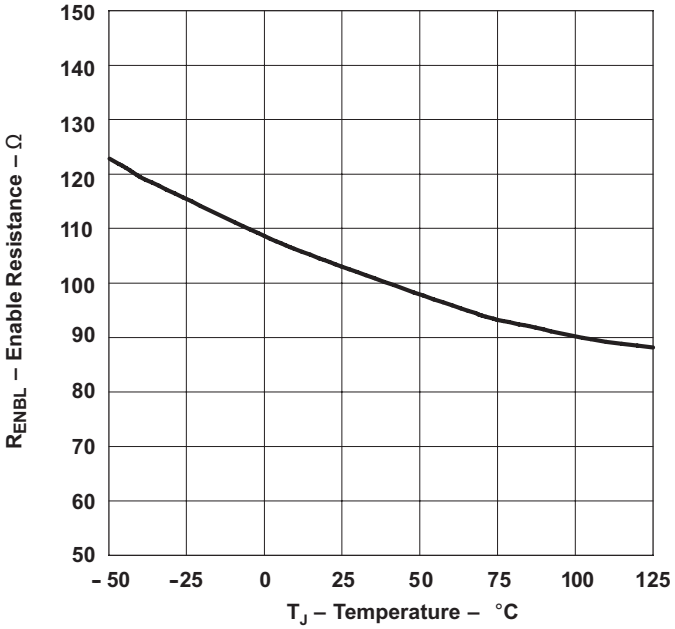


Figure 20.

TYPICAL CHARACTERICTICS (continued)

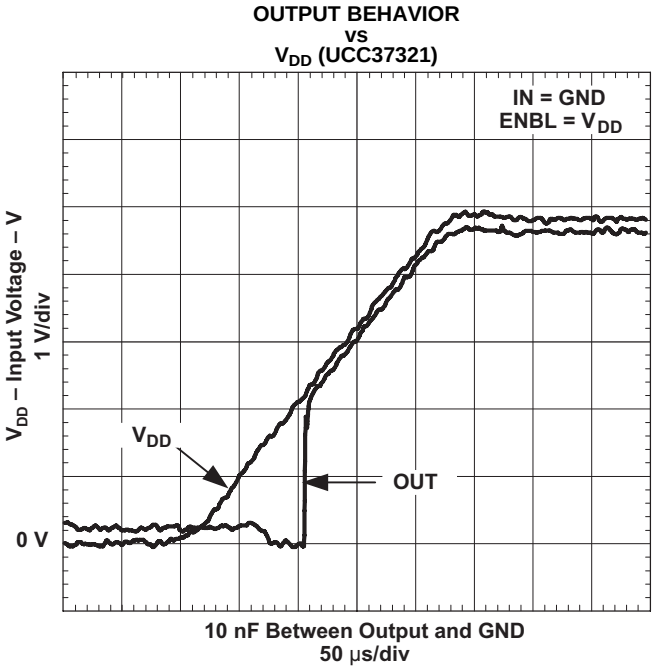


Figure 21.

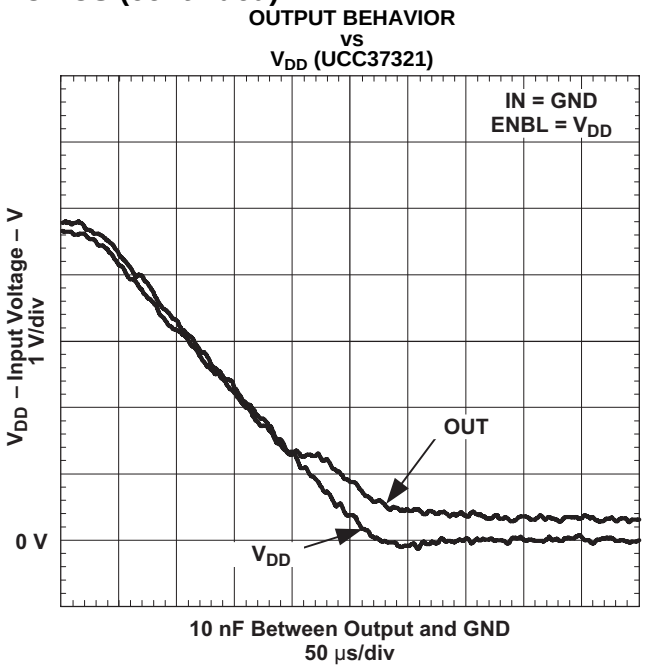


Figure 22.

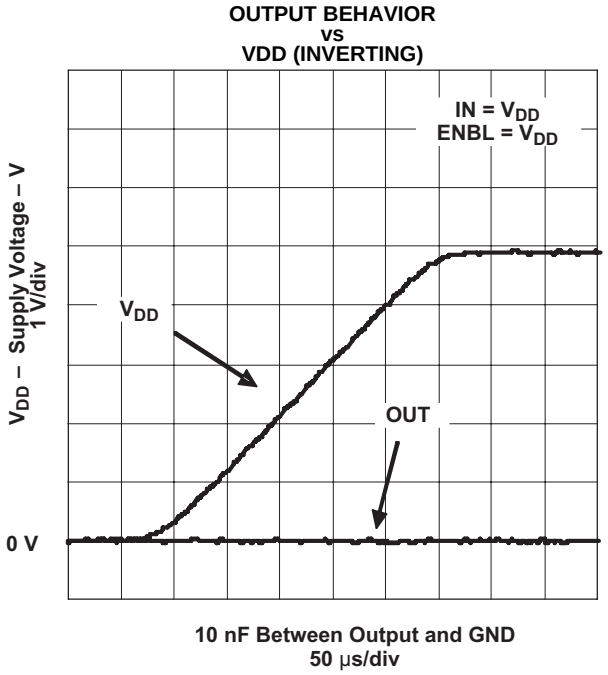


Figure 23.

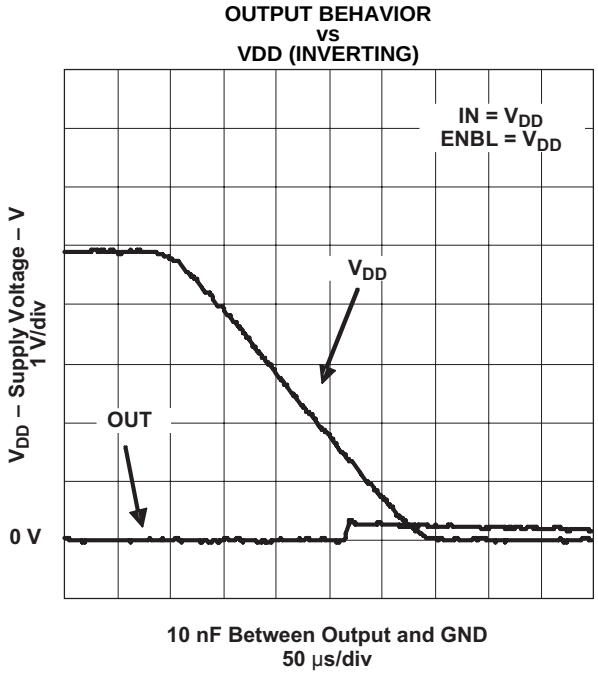


Figure 24.

TYPICAL CHARACTERICTICS (continued)

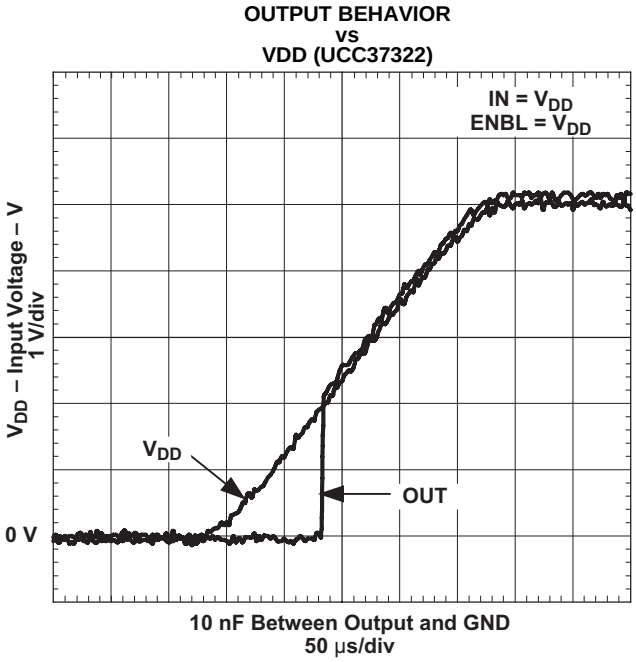


Figure 25.

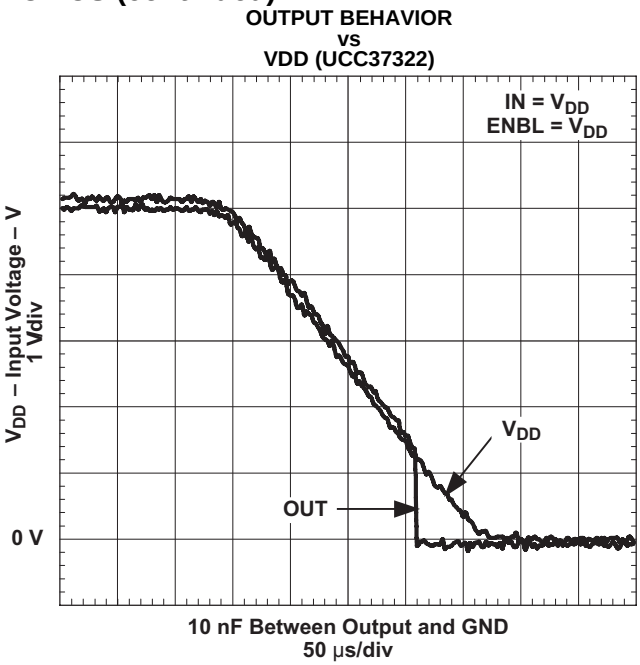


Figure 26.

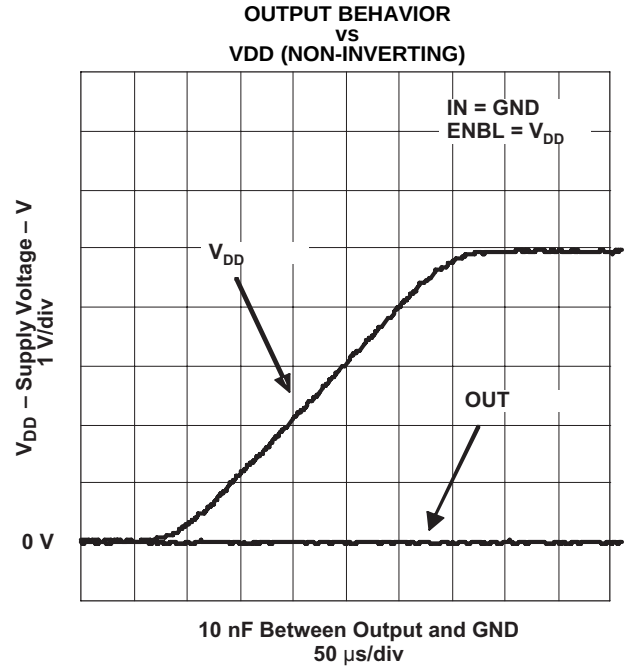


Figure 27.

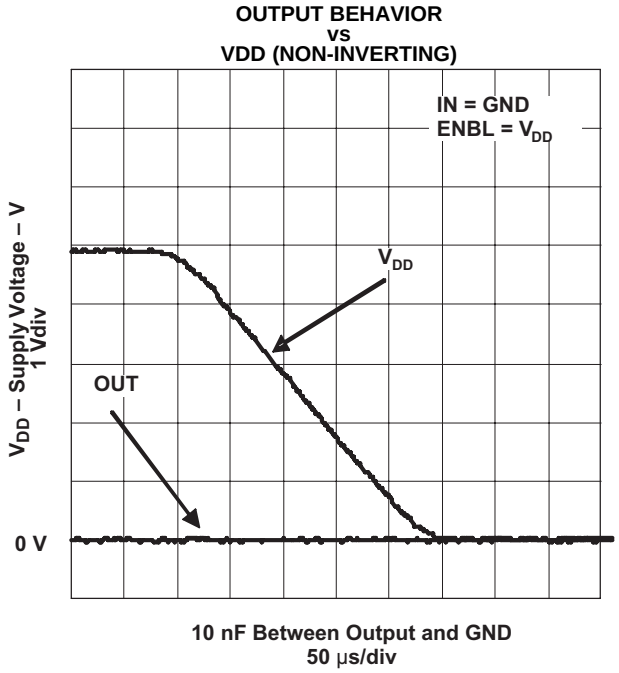


Figure 28.

REVISION HISTORY

DATE OF CHANGE	DESCRIPTION OF CHANGE
January, 2010	Updated AGND pin description.

Changes from Revision F (March 2012) to Revision G **Page**

- Changed minimum value for input voltage from –5 to –0.3 V in the *Absolute Maximum Ratings* table. 2
- Added C_{LOAD} = 10 nF to Fall Time vs Supply Voltage graph 12
- Changed Changed x-axis values from 1, 10, 100 to 0.1, 1, 10 in Rise Time vs Load Capacitance graph 13
- Changed Changed x-axis values from 1, 10, 100 to 0.1, 1, 10 in Fall Time vs Output Capacitance graph 13

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27321D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27321	Samples
UCC27321DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27321	Samples
UCC27321DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27321	Samples
UCC27321DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27321	Samples
UCC27321DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27321	Samples
UCC27321DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27321	Samples
UCC27321DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27321	Samples
UCC27321DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27321	Samples
UCC27321P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 105	UCC27321P	Samples
UCC27321PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 105	UCC27321P	Samples
UCC27322D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27322	Samples
UCC27322DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27322	Samples
UCC27322DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27322	Samples
UCC27322DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27322	Samples
UCC27322DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27322	Samples
UCC27322DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27322	Samples
UCC27322DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27322	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27322DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	27322	Samples
UCC27322P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 105	UCC27322P	Samples
UCC27322PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 105	UCC27322P	Samples
UCC37321D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37321	Samples
UCC37321DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37321	Samples
UCC37321DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37321	Samples
UCC37321DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37321	Samples
UCC37321DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37321	Samples
UCC37321DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37321	Samples
UCC37321DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37321	Samples
UCC37321DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37321	Samples
UCC37321P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC37321P	Samples
UCC37321PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC37321P	Samples
UCC37322D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37322	Samples
UCC37322DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37322	Samples
UCC37322DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37322	Samples
UCC37322DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37322	Samples
UCC37322DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37322	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC37322DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37322	Samples
UCC37322DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37322	Samples
UCC37322DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	37322	Samples
UCC37322P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC37322P	Samples
UCC37322PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC37322P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC27321, UCC27322 :

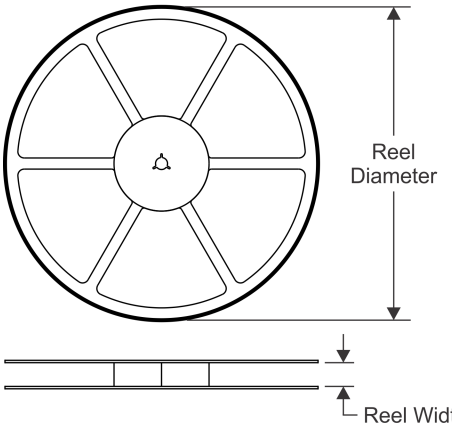
- Automotive: UCC27321-Q1, UCC27322-Q1
- Enhanced Product: UCC27322-EP

NOTE: Qualified Version Definitions:

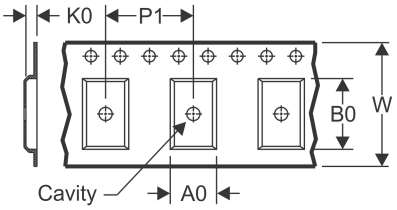
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

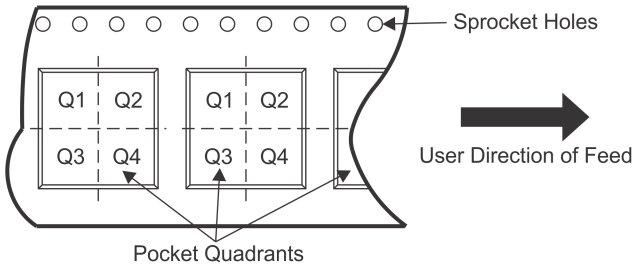


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

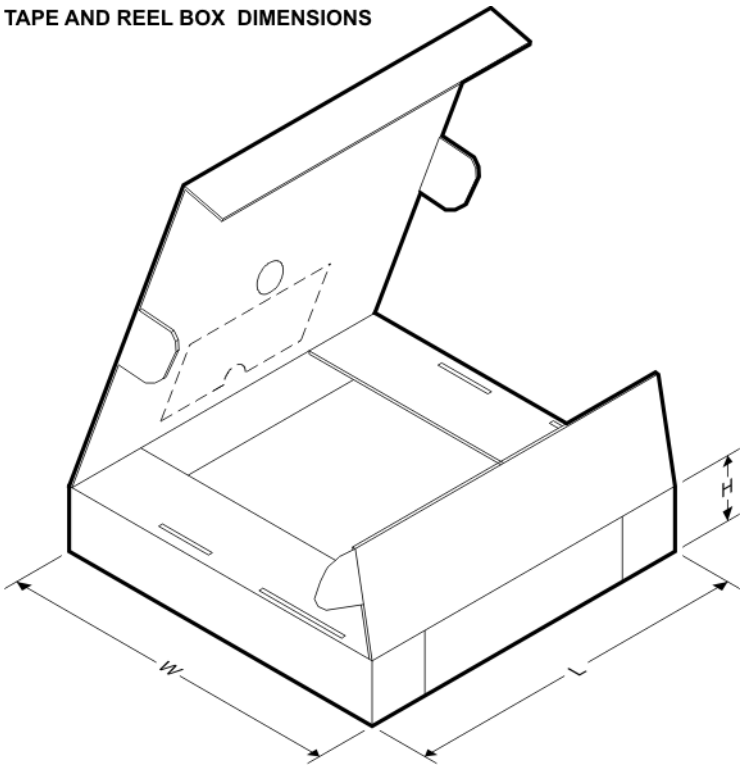
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27321DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27321DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27322DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27322DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37321DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37321DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37322DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37322DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

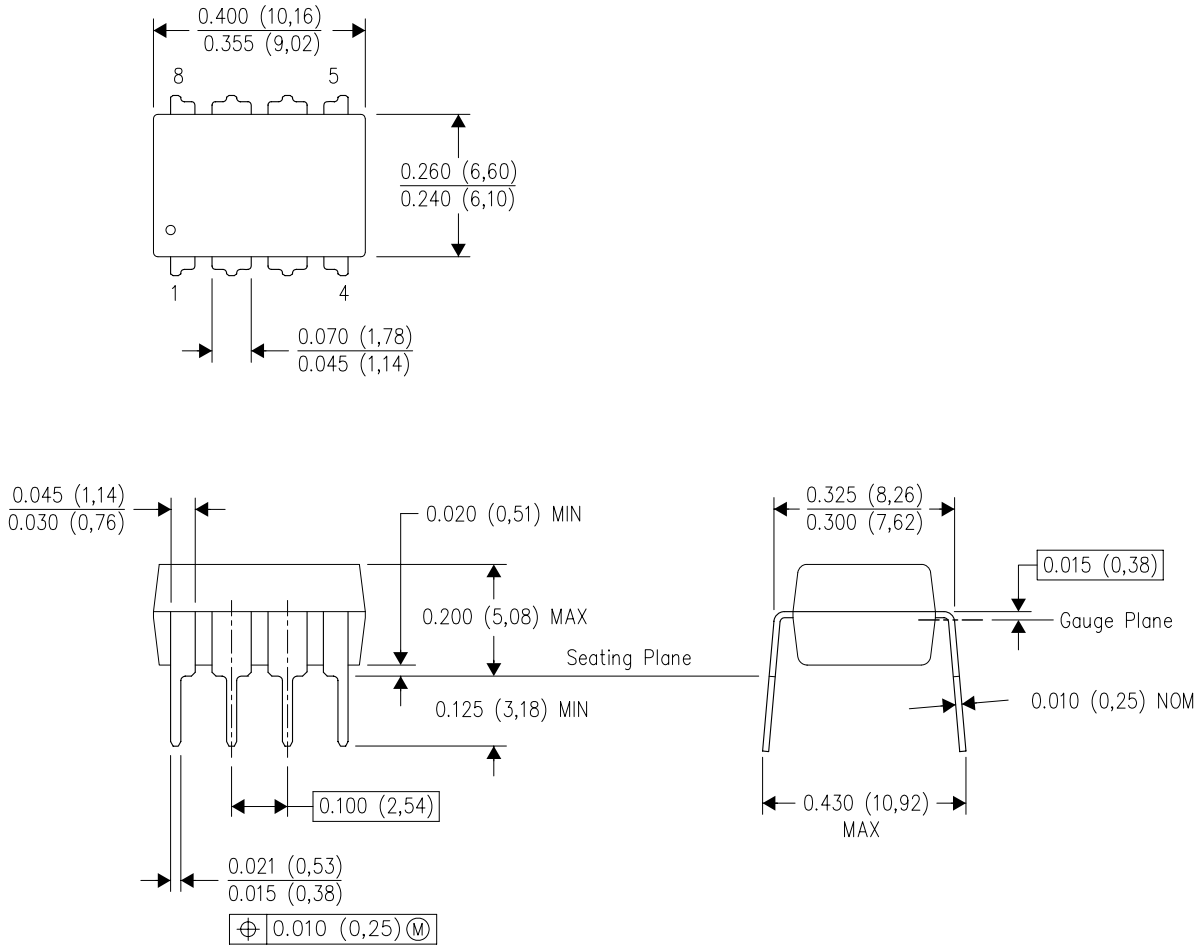
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

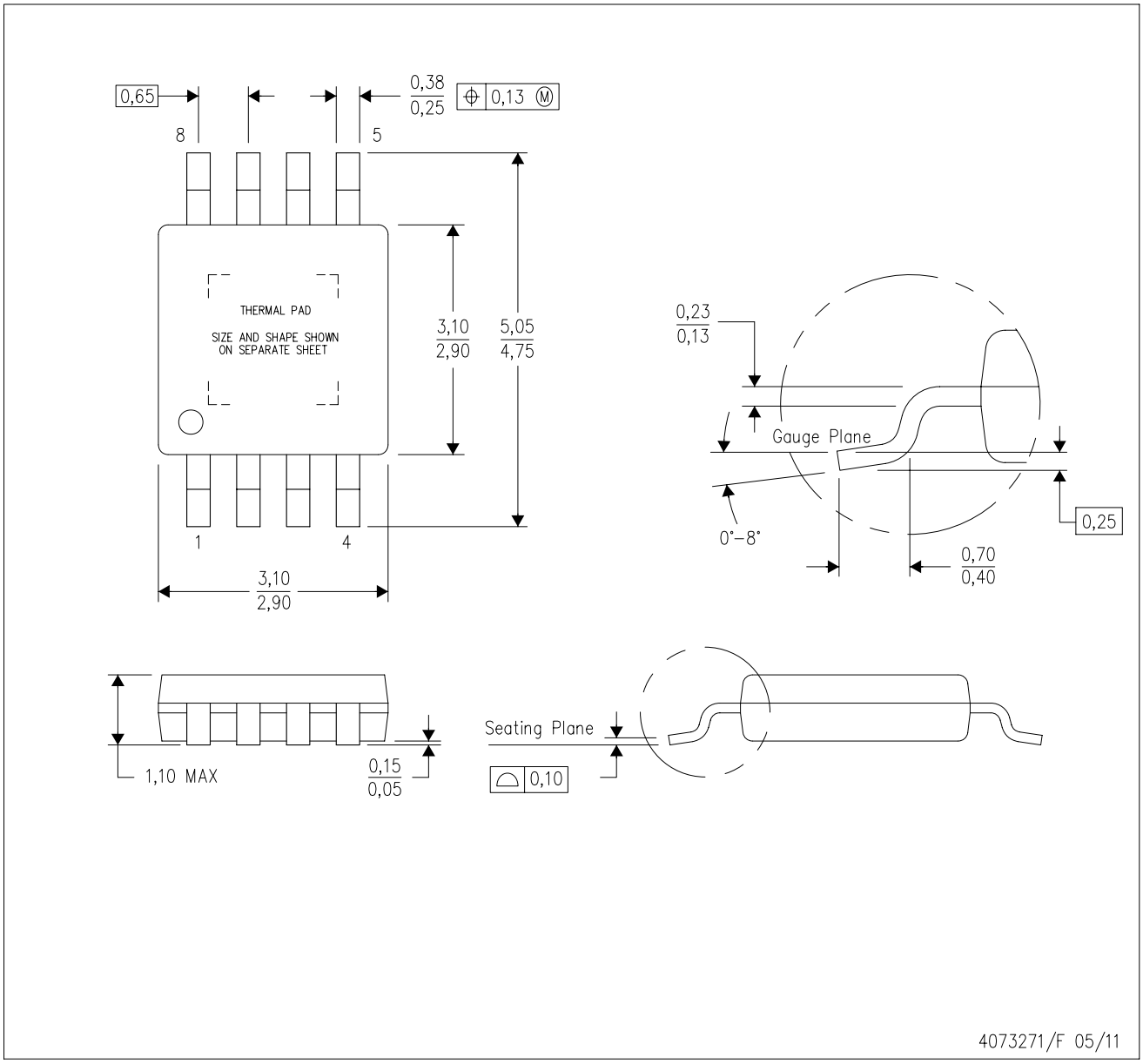
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27321DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
UCC27321DR	SOIC	D	8	2500	367.0	367.0	35.0
UCC27322DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
UCC27322DR	SOIC	D	8	2500	367.0	367.0	35.0
UCC37321DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
UCC37321DR	SOIC	D	8	2500	367.0	367.0	35.0
UCC37322DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
UCC37322DR	SOIC	D	8	2500	367.0	367.0	35.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

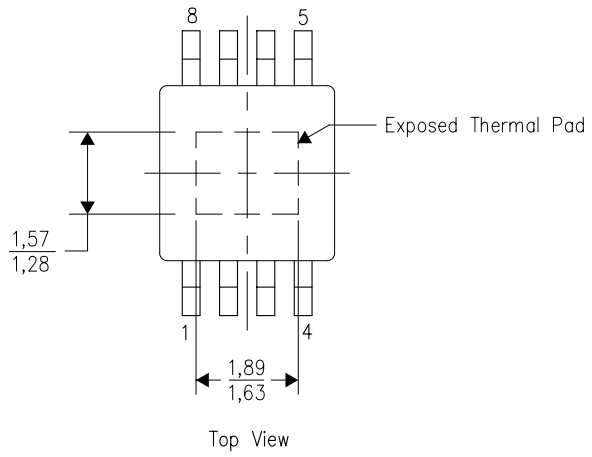
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

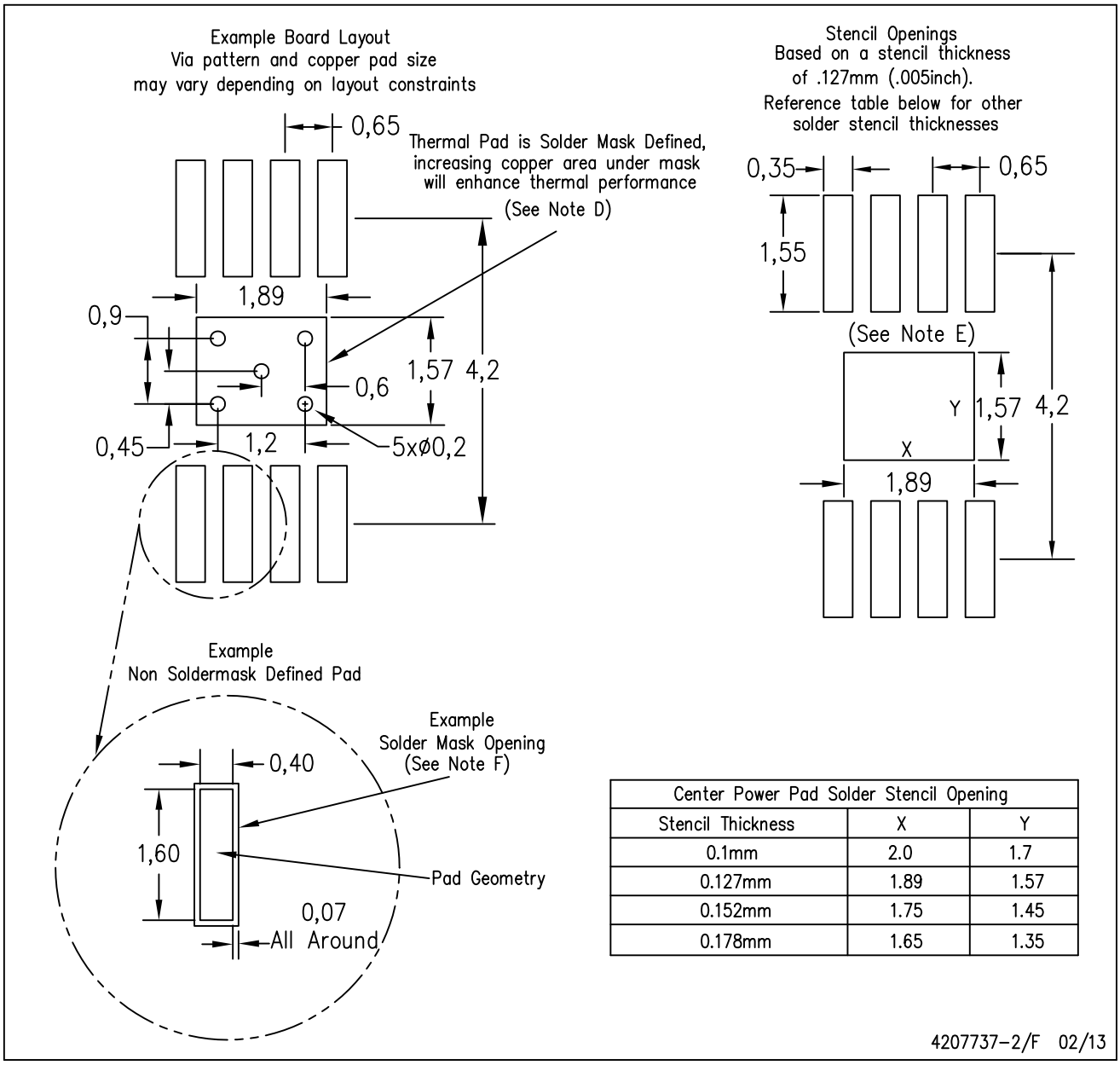
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

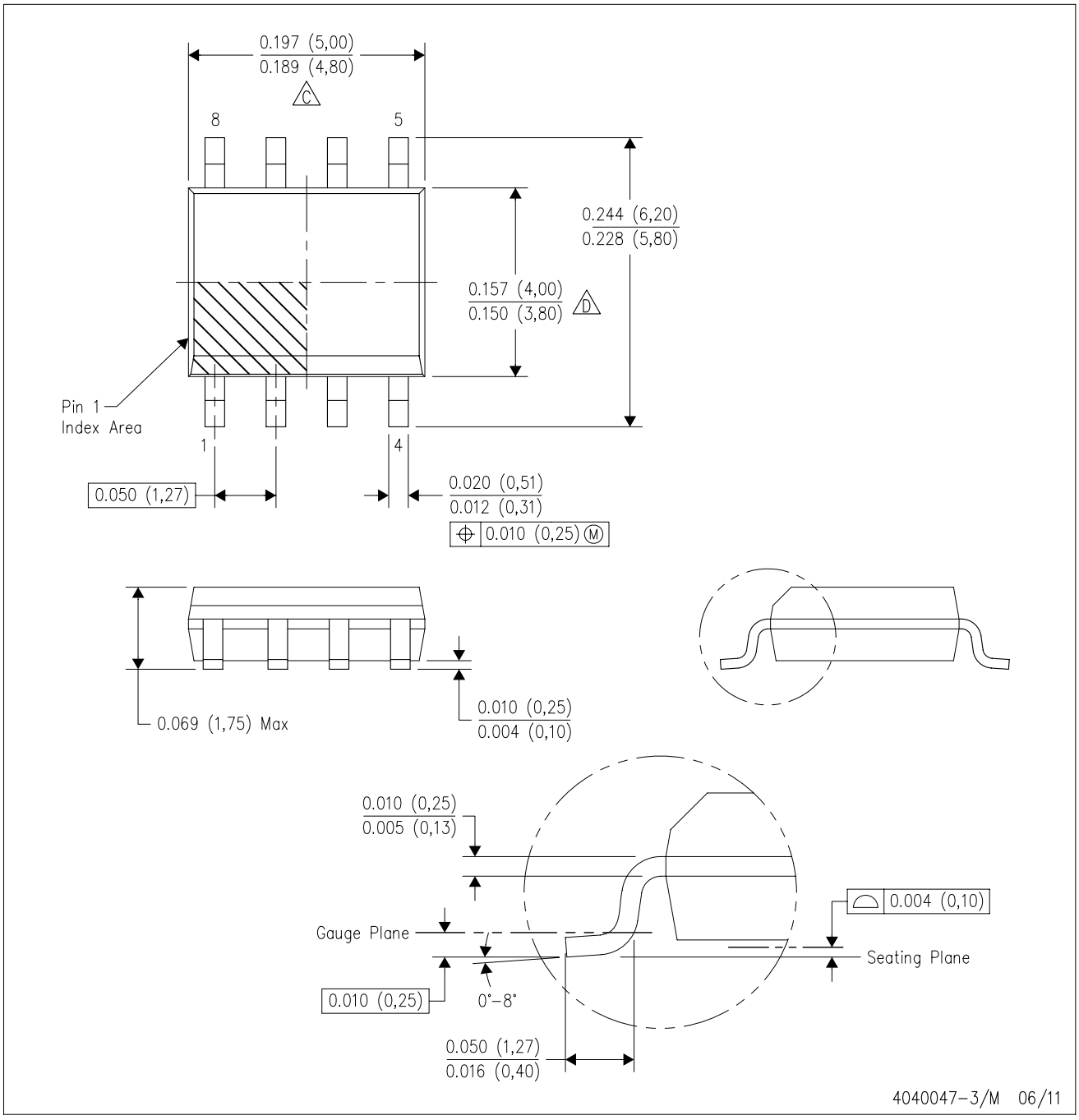


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

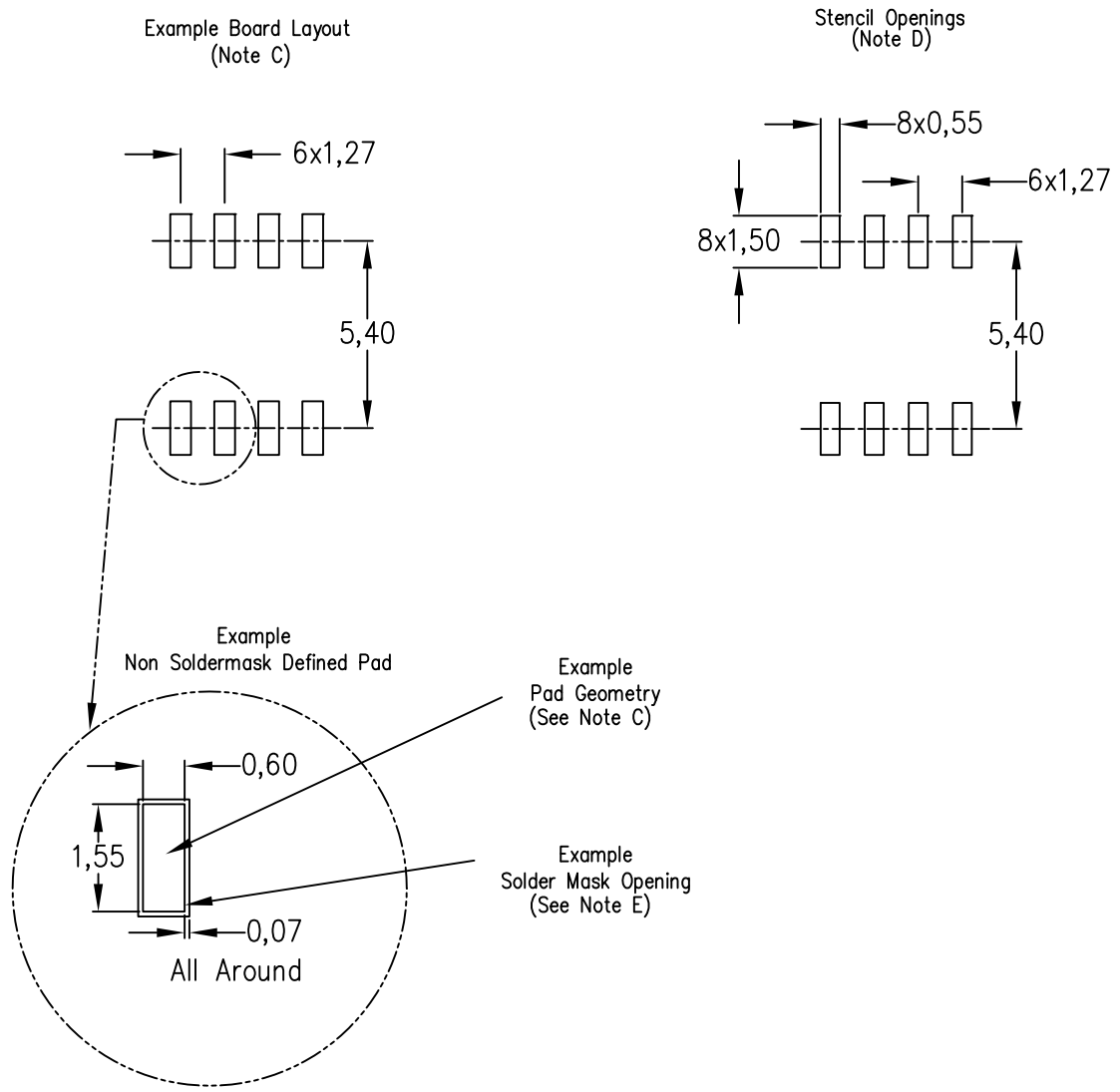
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265