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# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT139** Dual 2-to-4 line decoder/demultiplexer

Product specification  
File under Integrated Circuits, IC06

September 1993

## Dual 2-to-4 line decoder/demultiplexer

## 74HC/HCT139

## FEATURES

- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Active LOW mutually exclusive outputs
- Output capability: standard
- I<sub>CC</sub> category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT139 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT139 are high-speed, dual 2-to-4 line decoder/multiplexers. This device has two independent decoders, each accepting two binary weighted inputs ( $nA_0$  and  $nA_1$ ) and providing four mutually exclusive active LOW outputs ( $n\bar{Y}_0$  to  $n\bar{Y}_3$ ). Each decoder has an active LOW enable input ( $n\bar{E}$ ).

When  $n\bar{E}$  is HIGH, every output is forced HIGH. The enable can be used as the data input for a 1-to-4 demultiplexer application.

The "139" is identical to the HEF4556 of the HE4000B family.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

| SYMBOL                              | PARAMETER                                     | CONDITIONS                                    | TYPICAL |     | UNIT |
|-------------------------------------|---|---|---------|-----|------|
|                                     |   |   | HC      | HCT |      |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay                             | C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V |         |     |      |
|                                     | nA <sub>n</sub> to n $\bar{Y}_n$              |   | 11      | 13  | ns   |
|                                     | n $\bar{E}_3$ to n $\bar{Y}_n$                |   | 10      | 13  | ns   |
| C <sub>I</sub>                      | input capacitance                             |   | 3.5     | 3.5 | pF   |
| C <sub>PD</sub>                     | power dissipation capacitance per multiplexer | notes 1 and 2                                 | 42      | 44  | pF   |

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in  $\mu$ W):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> - 1.5 V

## APPLICATIONS

- Memory decoding or data-routing
- Code conversion

## ORDERING INFORMATION

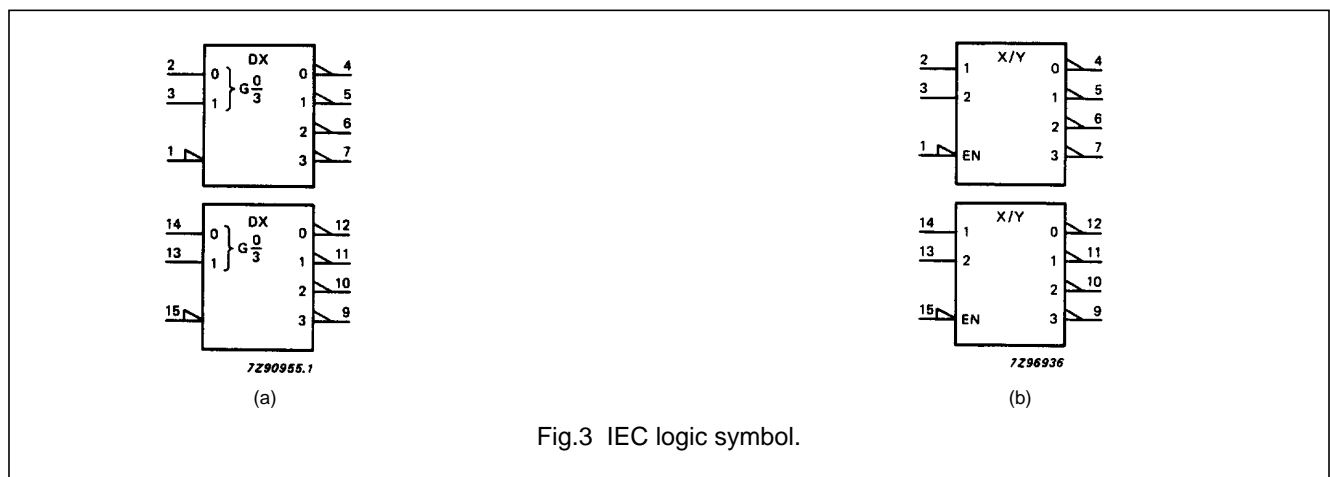
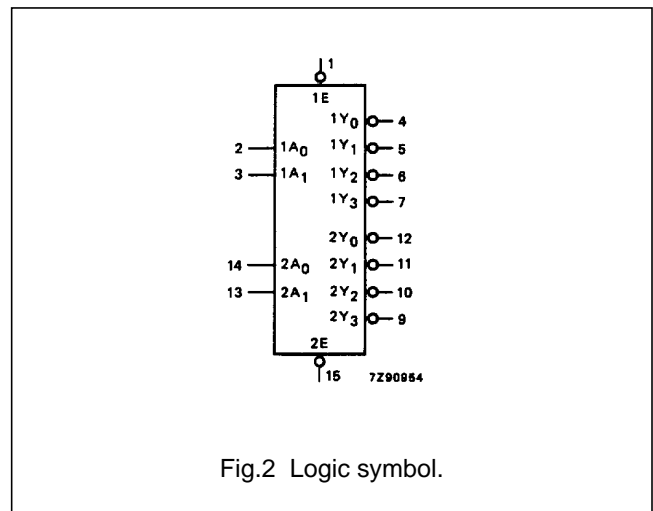
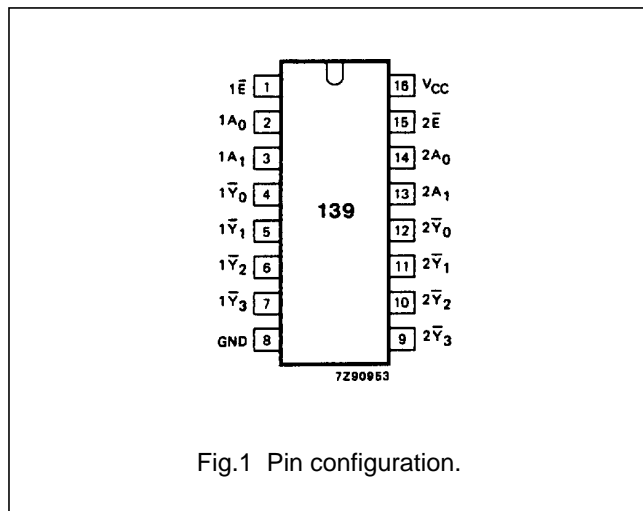
See "74HC/HCT/HCU/HCMOS Logic Package Information".

# Dual 2-to-4 line decoder/demultiplexer

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## PIN DESCRIPTION

| PIN NO.       | SYMBOL                       | NAME AND FUNCTION          |
|---------------|------------------------------|----------------------------|
| 1, 15         | $1\bar{E}, 2\bar{E}$         | enable inputs (active LOW) |
| 2, 3          | $1A_0, 1A_1$                 | address inputs             |
| 4, 5, 6, 7    | $1\bar{Y}_0$ to $1\bar{Y}_3$ | outputs (active LOW)       |
| 8             | GND                          | ground (0 V)               |
| 12, 11, 10, 9 | $2\bar{Y}_0$ to $2\bar{Y}_3$ | outputs (active LOW)       |
| 14, 13        | $2A_0, 2A_1$                 | address inputs             |
| 16            | $V_{CC}$                     | positive supply voltage    |



Dual 2-to-4 line decoder/demultiplexer

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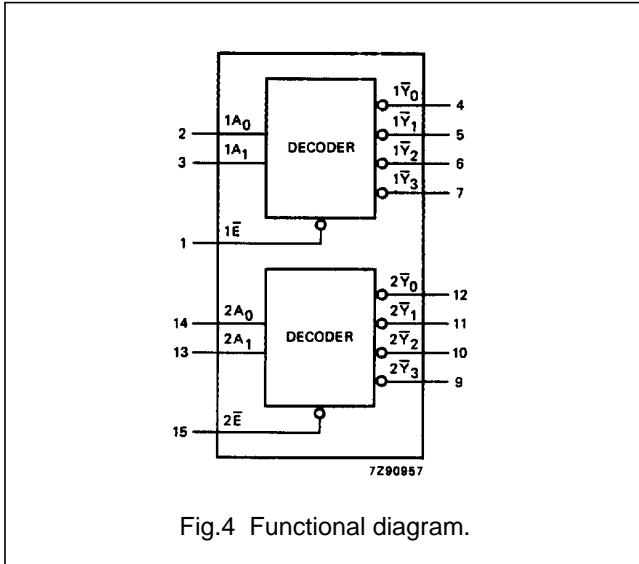


Fig.4 Functional diagram.

FUNCTION TABLE

| INPUTS     |        |        | OUTPUTS      |              |              |              |
|------------|--------|--------|--------------|--------------|--------------|--------------|
| $n\bar{E}$ | $nA_0$ | $nA_1$ | $n\bar{Y}_0$ | $n\bar{Y}_1$ | $n\bar{Y}_2$ | $n\bar{Y}_3$ |
| H          | X      | X      | H            | H            | H            | H            |
| L          | L      | L      | L            | H            | H            | H            |
| L          | H      | L      | H            | L            | H            | H            |
| L          | L      | H      | H            | H            | L            | H            |
| L          | H      | H      | H            | H            | H            | L            |

Notes

- 1. H = HIGH voltage level
- L = LOW voltage level
- X = don't care

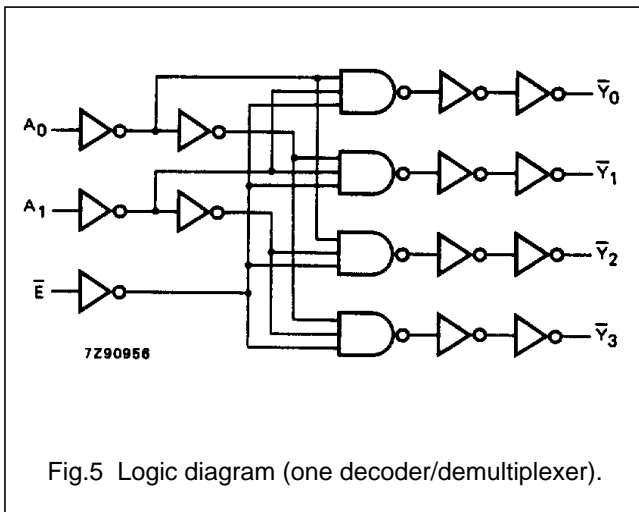


Fig.5 Logic diagram (one decoder/demultiplexer).

## Dual 2-to-4 line decoder/demultiplexer

## 74HC/HCT139

**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**AC CHARACTERISTICS FOR 74HC**

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER   | T <sub>amb</sub> (°C) |                |                 |            |                 |             | UNIT            | TEST CONDITIONS        |                   |              |
|-------------------------------------|---|-----------------------|----------------|-----------------|------------|-----------------|-------------|-----------------|------------------------|-------------------|--------------|
|                                     |   | 74HC                  |                |                 |            |                 |             |                 | V <sub>CC</sub><br>(V) | WAVEFORMS         |              |
|                                     |   | +25                   |                |                 | -40 to +85 |                 | -40 to +125 |                 |                        |                   |              |
|                                     |   | min.                  | typ.           | max.            | min.       | max.            | min.        |                 |                        |                   | max.         |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nA <sub>n</sub> to $\bar{Y}_n$ |                       | 39<br>14<br>11 | 145<br>29<br>25 |            | 180<br>36<br>31 |             | 220<br>44<br>38 | ns                     | 2.0<br>4.5<br>6.0 | Fig.6        |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>n $\bar{E}$ to n $\bar{Y}_n$   |                       | 33<br>12<br>10 | 135<br>27<br>23 |            | 170<br>34<br>29 |             | 205<br>41<br>35 | ns                     | 2.0<br>4.5<br>6.0 | Fig.7        |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition<br>time                           |                       | 19<br>7<br>6   | 75<br>15<br>13  |            | 95<br>19<br>16  |             | 110<br>22<br>19 | ns                     | 2.0<br>4.5<br>6.0 | Figs 6 and 7 |

## Dual 2-to-4 line decoder/demultiplexer

## 74HC/HCT139

**DC CHARACTERISTICS FOR HCT**

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

**Note to HCT types**

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT           | UNIT LOAD COEFFICIENT |
|-----------------|-----------------------|
| 1A <sub>n</sub> | 0.70                  |
| 2A <sub>n</sub> | 0.70                  |
| n $\bar{E}$     | 1.35                  |

**AC CHARACTERISTICS FOR 74HCT**

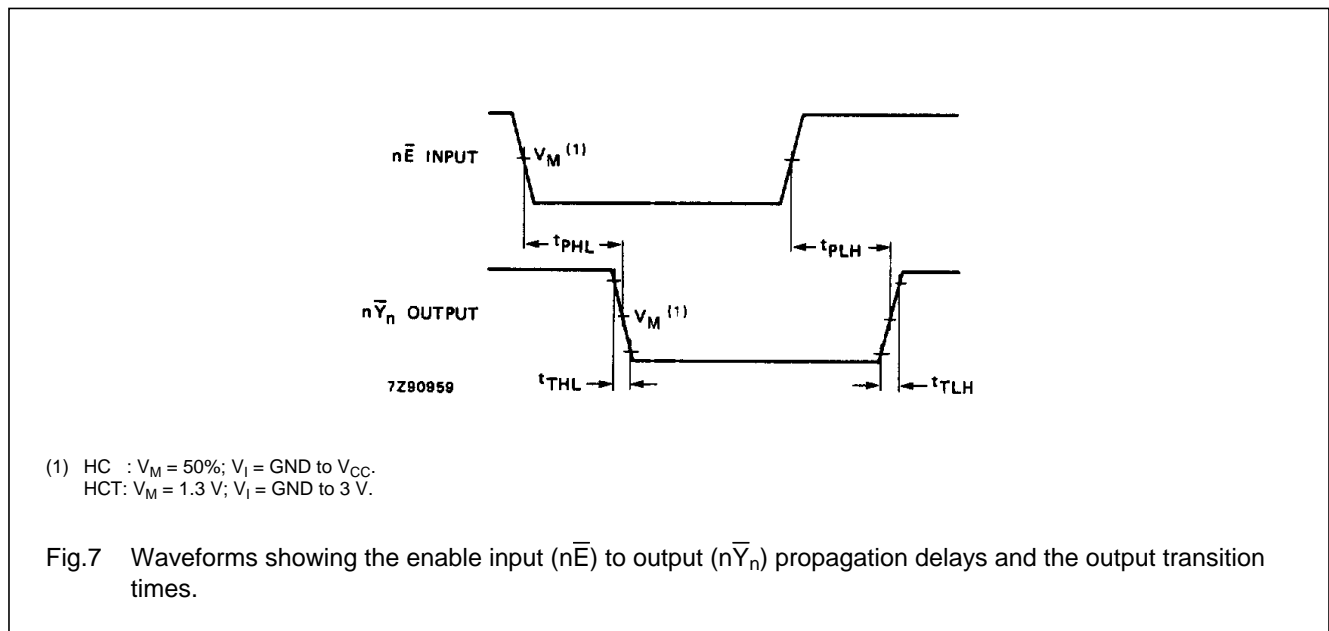
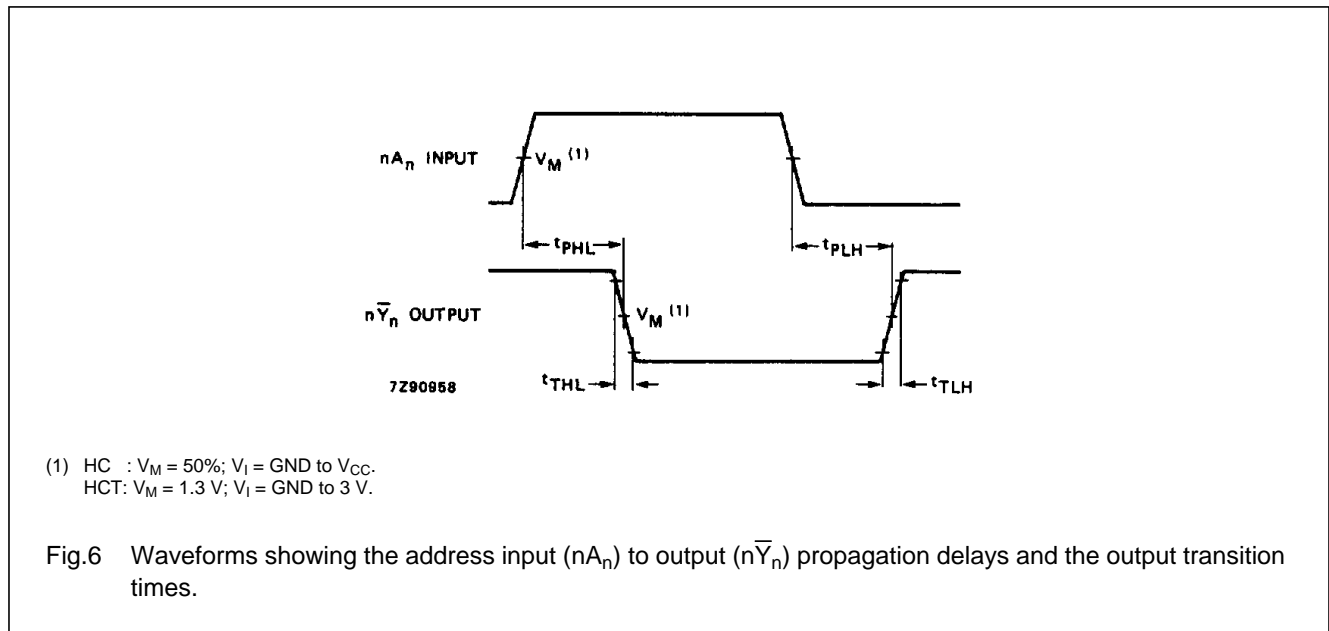
GND = 0 V; t<sub>f</sub> = t<sub>r</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER   | T <sub>amb</sub> (°C) |      |      |            |      |             |      |    | UNIT | TEST CONDITIONS        |           |
|-------------------------------------|---|-----------------------|------|------|------------|------|-------------|------|----|------|------------------------|-----------|
|                                     |   | 74HCT                 |      |      |            |      |             |      |    |      | V <sub>CC</sub><br>(V) | WAVEFORMS |
|                                     |   | +25                   |      |      | -40 to +85 |      | -40 to +125 |      |    |      |                        |           |
|                                     |   | min.                  | typ. | max. | min.       | max. | min.        | max. |    |      |                        |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>nA <sub>n</sub> to $\bar{Y}_n$ |                       | 16   | 34   |            | 43   |             | 51   | ns | 4.5  | Fig.6                  |           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>n $\bar{E}$ to n $\bar{Y}_n$   |                       | 16   | 34   |            | 43   |             | 51   | ns | 4.5  | Fig.7                  |           |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition<br>time                           |                       | 7    | 15   |            | 19   |             | 22   | ns | 4.5  | Figs 6 and 7           |           |

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".