



HESTORE.HU

elektronikai alkatrész áruház

EN: This Datasheet is presented by the manufacturer.

Please visit our website for pricing and availability at www.hestore.hu.

μ A741 General-Purpose Operational Amplifiers

1 Features

- Short-Circuit Protection
- Offset-Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- No Frequency Compensation Required
- No Latch-Up

2 Applications

- DVD Recorders and Players
- Pro Audio Mixers

3 Description

The μ A741 device is a general-purpose operational amplifier featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in [Figure 11](#).

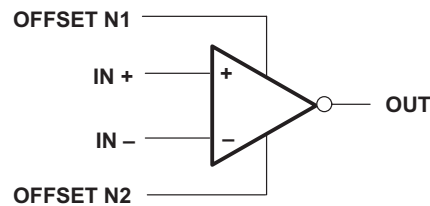
The μ A741C device is characterized for operation from 0°C to 70°C. The μ A741M device (obsolete) is characterized for operation over the full military temperature range of –55°C to 125°C.

Device Information⁽¹⁾

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
μ A741x	SOIC (8)	4.90 mm x 3.91 mm
	PDIP (8)	9.81 mm x 6.35 mm
	SO (8)	6.20 mm x 5.30 mm

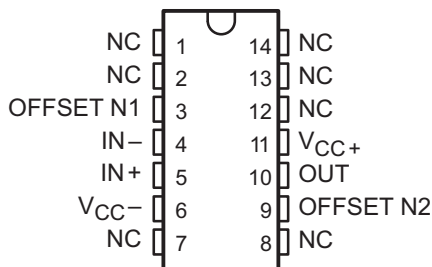
(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

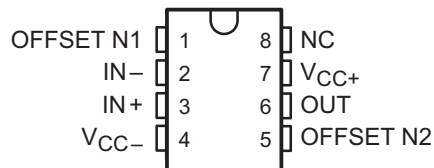


6 Pin Configurations and Functions

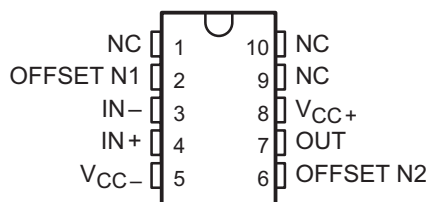
μA741M . . . J PACKAGE
(TOP VIEW)



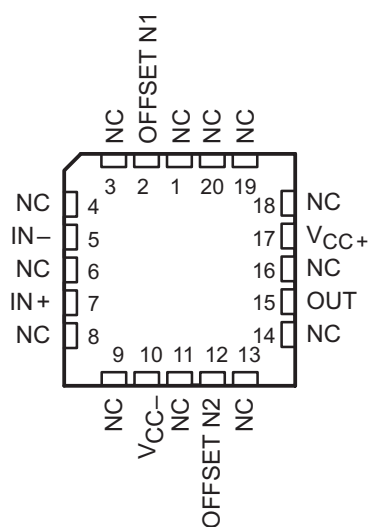
μA741M . . . JG PACKAGE
μA741C, μA741I . . . D, P, OR PW PACKAGE
(TOP VIEW)



μA741M . . . U PACKAGE
(TOP VIEW)



μA741M . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

Pin Functions

NAME	PIN				TYPE	DESCRIPTION
	J	JG, D, P, or PW	U	FK		
IN+	5	3	4	7	I	Noninverting input
IN-	4	2	3	5	I	Inverting input
NC	1, 2, 8, 12, 13, 14	8	1, 9, 10	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19, 20	—	Do not connect
OFFSET N1	3	1	2	2	I	External input offset voltage adjustment
OFFSET N2	9	5	6	12	I	External input offset voltage adjustment
OUT	10	6	7	15	O	Output
V _{CC} +	11	7	8	17	—	Positive supply
V _{CC} -	6	4	5	10	—	Negative supply

7 Specifications

7.1 Absolute Maximum Ratings

 over virtual junction temperature range (unless otherwise noted)⁽¹⁾

		μA741C		μA741M		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage ⁽²⁾	-18	18	-22	22	C
V_{ID}	Differential input voltage ⁽³⁾	-15	15	-30	30	V
V_I	Input voltage, any input ⁽²⁾⁽⁴⁾	-15	15	-15	15	V
	Voltage between offset null (either OFFSET N1 or OFFSET N2) and V_{CC-}	-15	15	-0.5	0.5	V
	Duration of output short circuit ⁽⁵⁾	Unlimited				
	Continuous total power dissipation	See Table 1				
T_A	Operating free-air temperature range	0	70	-55	125	°C
	Case temperature for 60 seconds	FK package		260		°C
	Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J, JG, or U package		300		°C
	Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds	D, P, or PS package		N/A	N/A	°C
T_{stg}	Storage temperature range	-65	150	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, unless otherwise noted, are with respect to the midpoint between V_{CC+} and V_{CC-} .
- (3) Differential voltages are at $IN+$ with respect to $IN-$.
- (4) The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 V, whichever is less.
- (5) The output may be shorted to ground or either power supply. For the μA741M only, the unlimited duration of the short circuit applies at (or below) 125°C case temperature or 75°C free-air temperature.

7.2 Recommended Operating Conditions

		MIN	MAX	UNIT	
V_{CC+}	Supply voltage	5	15	V	
V_{CC-}		-5	-15		
T_A	Operating free-air temperature	μA741C	0	70	°C
		μA741M	-55	125	

Table 1. Dissipation Ratings Table

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	DERATE ABOVE T_A	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	500 mW	5.8 mW/°C	64°C	464 mW	377 mW	N/A
FK	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
J	500 mW	11.0 mW/°C	105°C	500 mW	500 mW	275 mW
JG	500 mW	8.4 mW/°C	90°C	500 mW	500 mW	210 mW
P	500 mW	N/A	N/A	500 mW	500 mW	N/A
PS	525 mW	4.2 mW/°C	25°C	336 mW	N/A	N/A
U	500 mW	5.4 mW/°C	57°C	432 mW	351 mW	135 mW

7.3 Electrical Characteristics μ A741C, μ A741M

 at specified virtual junction temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A ⁽¹⁾	μ A741C			μ A741M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_O = 0$	25°C	1		6	1		5	mV
		Full range			7.5	± 15		6	
$\Delta V_{IO(adj)}$ Offset voltage adjust range	$V_O = 0$	25°C	± 15			20	200	mV	
I_{IO} Input offset current	$V_O = 0$	25°C	20	200	500			nA	
		Full range	300			500			
I_{IB} Input bias current	$V_O = 0$	25°C	80	500	80		500	nA	
		Full range	800			1500			
V_{ICR} Common-mode input voltage range		25°C	± 12	± 13	± 12		± 13	V	
		Full range	± 12		± 12				
V_{OM} Maximum peak output voltage swing	$R_L = 10$ k Ω	25°C	± 12	± 14	± 12		± 14	V	
	$R_L \geq 10$ k Ω	Full range	± 12		± 12				
	$R_L = 2$ k Ω	25°C	± 10		± 10		± 13		
	$R_L \geq 2$ k Ω	Full range	± 10		± 10				
A_{VD} Large-signal differential voltage amplification	$R_L \geq 2$ k Ω	25°C	20	200	50	200	V/mV		
	$V_O = \pm 10$ V	Full range	15		25				
r_i Input resistance		25°C	0.3	2	0.3	2	M Ω		
r_o Output resistance	$V_O = 0$, See ⁽²⁾	25°C	75		75		Ω		
C_i Input capacitance		25°C	1.4		1.4		pF		
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$	25°C	70	90	70	90	dB		
		Full range	70		70				
k_{SVS} Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ± 15 V	25°C	30	150	30	150	μ V/V		
		Full range	150		150				
I_{OS} Short-circuit output current		25°C	± 25	± 40	± 25	± 40	mA		
I_{CC} Supply current	$V_O = 0$, No load	25°C	1.7	2.8	1.7	2.8	mA		
		Full range	3.3		3.3				
P_D Total power dissipation	$V_O = 0$, No load	25°C	50	85	50	85	mW		
		Full range	100		100				

- (1) All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Full range for the μ A741C is 0°C to 70°C and the μ A741M is –55°C to 125°C.
- (2) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

7.4 Electrical Characteristics μ A741Y

at specified virtual junction temperature, $V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted) ⁽¹⁾

PARAMETER		TEST CONDITIONS	μ A741Y			UNIT
			MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_O = 0$		1	5	mV
$\Delta V_{IO(adj)}$	Offset voltage adjust range	$V_O = 0$		± 15		mV
I_{IO}	Input offset current	$V_O = 0$		20	200	nA
I_{IB}	Input bias current	$V_O = 0$		80	500	nA
V_{ICR}	Common-mode input voltage range		± 12	± 13		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10$ k Ω	± 12	± 14		V
		$R_L = 2$ k Ω	± 10	± 13		
A_{VD}	Large-signal differential voltage amplification	$R_L \geq 2$ k Ω	20	200		V/mV
r_i	Input resistance		0.3	2		M Ω
r_o	Output resistance	$V_O = 0$, See ⁽¹⁾		75		Ω
C_i	Input capacitance			1.4		pF
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$	70	90		dB
k_{SVS}	Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$)	$V_{CC} = \pm 9$ V to ± 15 V		30	150	μ V/V
I_{OS}	Short-circuit output current			± 25	± 40	mA
I_{CC}	Supply current	$V_O = 0$, No load		1.7	2.8	mA
P_D	Total power dissipation	$V_O = 0$, No load		50	85	mW

(1) This typical value applies only at frequencies above a few hundred hertz because of the effects of drift and thermal feedback.

7.5 Switching Characteristics μ A741C, μ A741M

over operating free-air temperature range, $V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	μ A741C			μ A741M			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ k Ω , $C_L = 100$ pF, See Figure 1		0.3			0.3		μ s
	Overshoot factor			5%			5%		—
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ k Ω , $C_L = 100$ pF, See Figure 1		0.5			0.5		V/ μ s

7.6 Switching Characteristics μ A741Y

over operating free-air temperature range, $V_{CC\pm} = \pm 15$ V, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	μ A741Y			UNIT
			MIN	TYP	MAX	
t_r	Rise time	$V_I = 20$ mV, $R_L = 2$ k Ω , $C_L = 100$ pF, See Figure 1		0.3		μ s
	Overshoot factor			5%		—
SR	Slew rate at unity gain	$V_I = 10$ V, $R_L = 2$ k Ω , $C_L = 100$ pF, See Figure 1		0.5		V/ μ s

7.7 Typical Characteristics

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

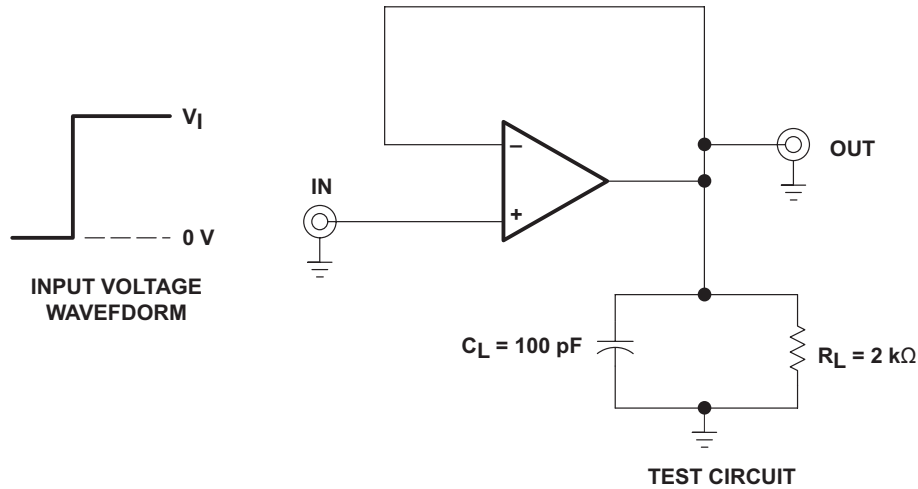


Figure 1. Rise Time, Overshoot, and Slew Rate

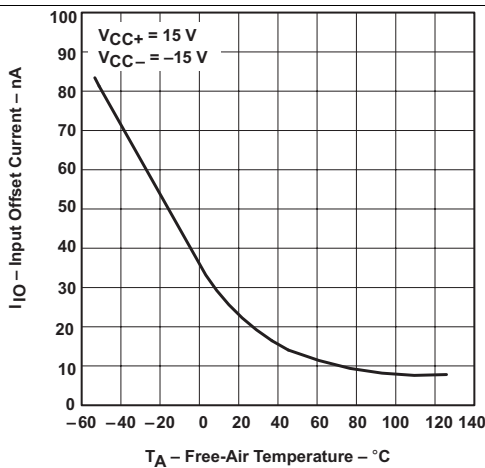


Figure 2. Input Offset Current vs Free-Air Temperature

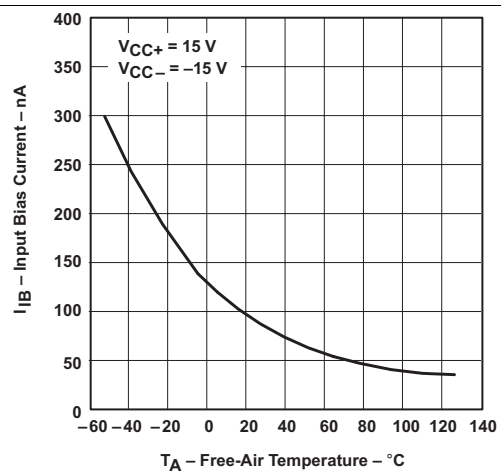


Figure 3. Input Bias Current vs Free-Air Temperature

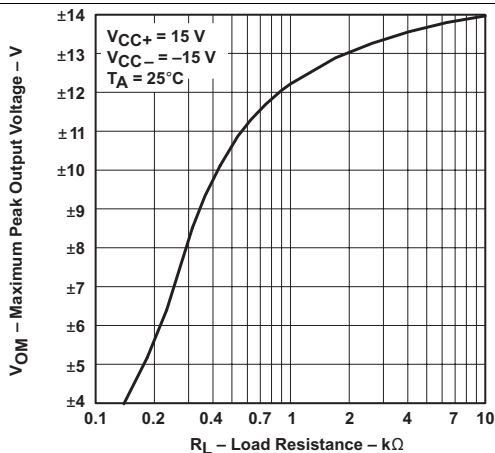


Figure 4. Maximum Output Voltage vs Load Resistance

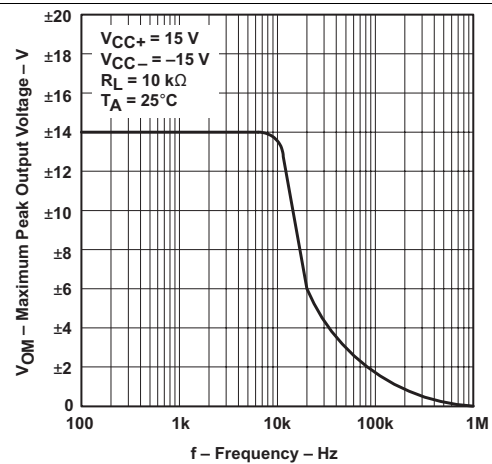


Figure 5. Maximum Peak Output Voltage vs Frequency

Typical Characteristics (continued)

Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

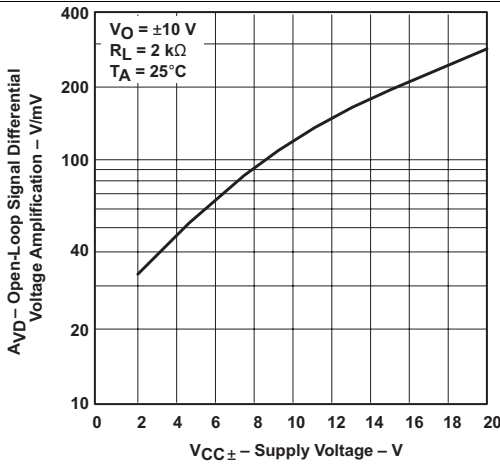


Figure 6. Open-Loop Signal Differential Voltage Amplification vs Supply Voltage

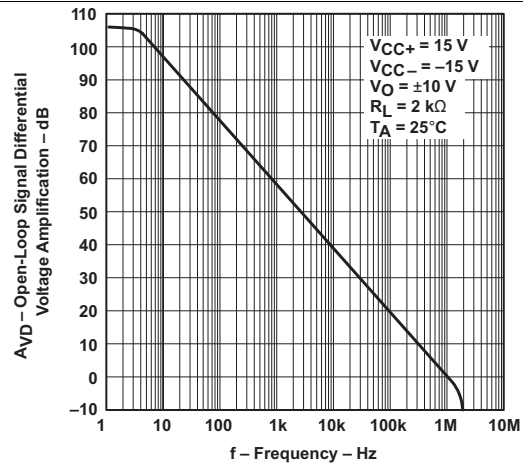


Figure 7. Open-Loop Large-Signal Differential Voltage Amplification vs Frequency

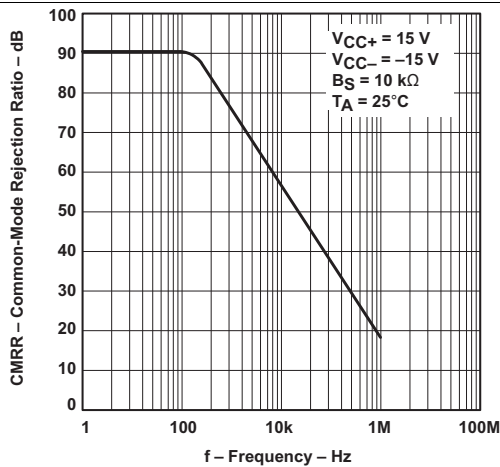


Figure 8. Common-Mode Rejection Ratio vs Frequency

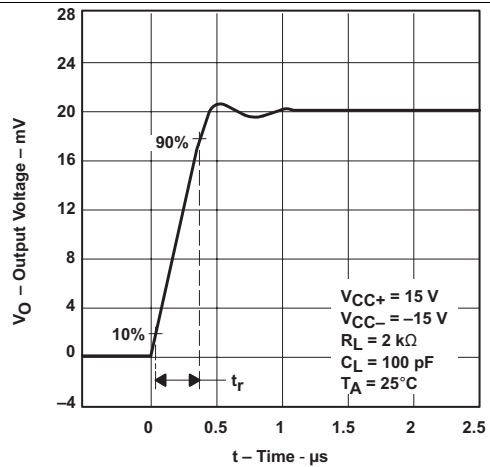


Figure 9. Output Voltage vs Elapsed Time

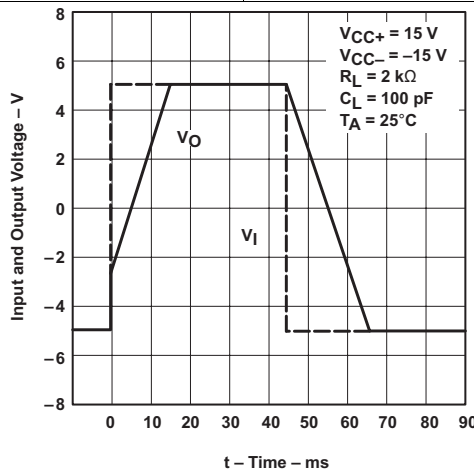


Figure 10. Voltage-Follower Large-Signal Pulse Response

8 Detailed Description

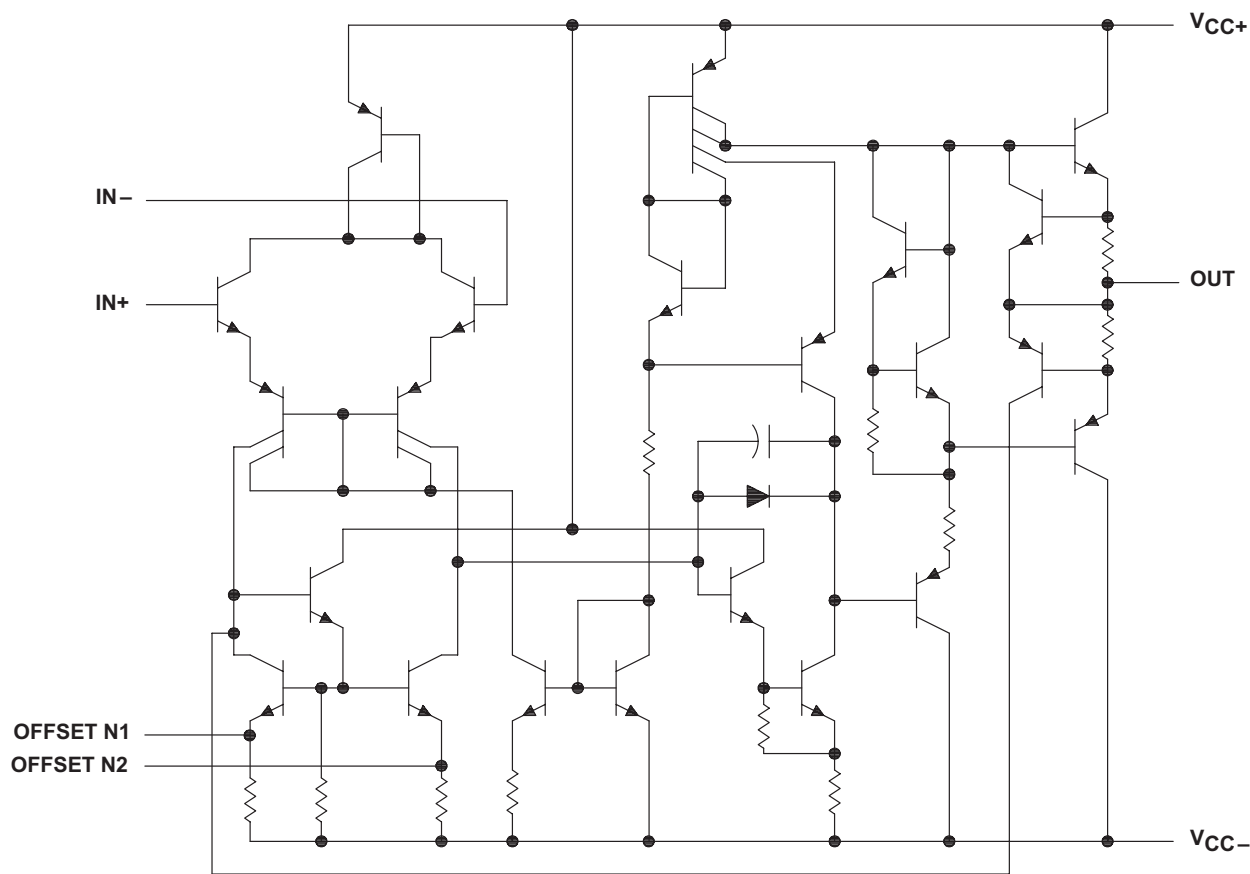
8.1 Overview

The μ A741 device is a general-purpose operational amplifier featuring offset-voltage null capability.

The high common-mode input voltage range and the absence of latch-up make the amplifier ideal for voltage-follower applications. The device is short-circuit protected and the internal frequency compensation ensures stability without external components. A low value potentiometer may be connected between the offset null inputs to null out the offset voltage as shown in [Figure 11](#).

The μ A741C device is characterized for operation from 0°C to 70°C. The μ A741M device (obsolete) is characterized for operation over the full military temperature range of –55°C to 125°C.

8.2 Functional Block Diagram



Component Count	
Transistors	22
Resistors	11
Diode	1
Capacitor	1

8.3 Feature Description

8.3.1 Offset-Voltage Null Capability

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors, etc. The input offset pins allow the designer to adjust for these mismatches by external circuitry. See the [Application and Implementation](#) section for more details on design techniques.

8.3.2 Slew Rate

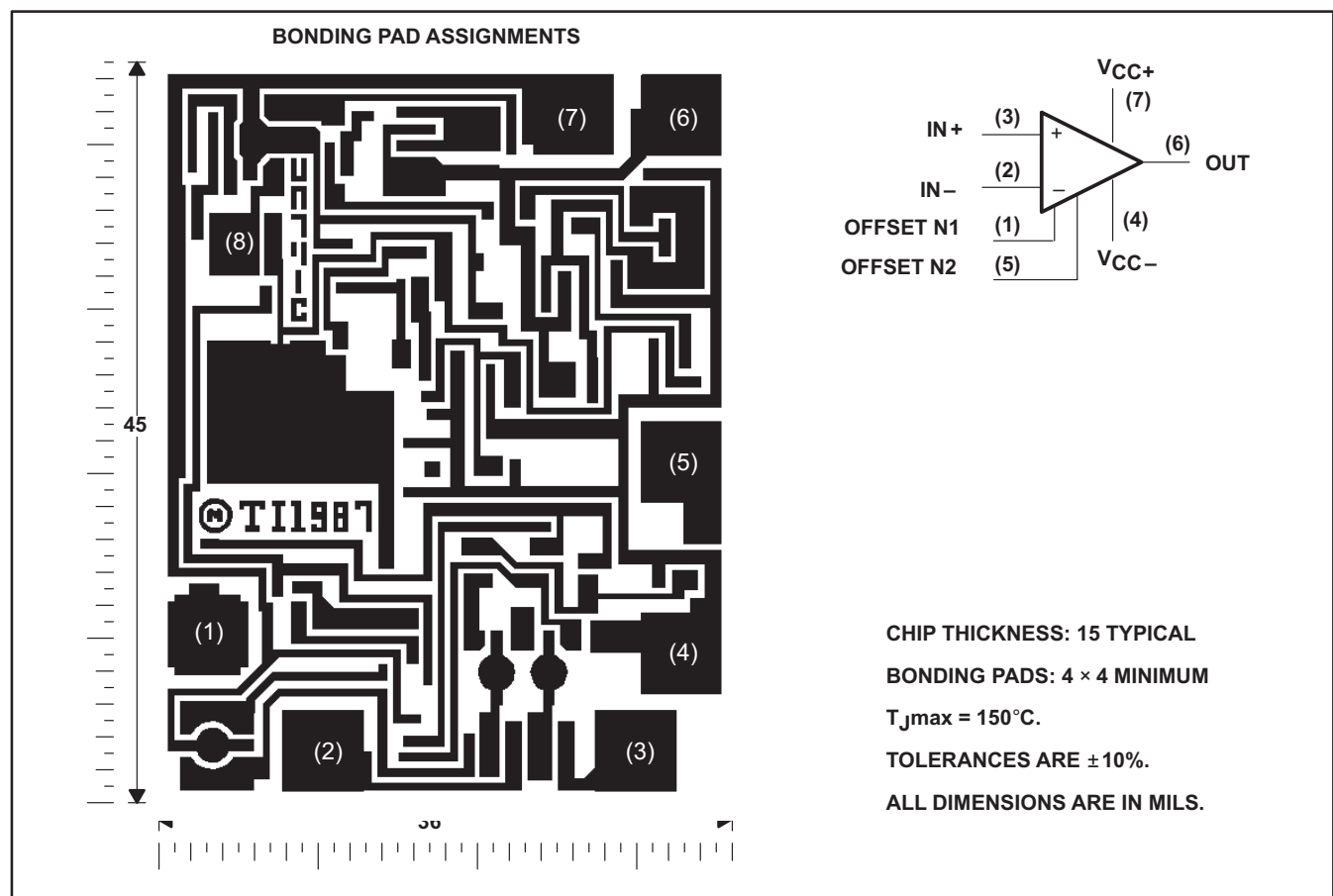
The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The μ A741 has a 0.5-V/ μ s slew rate. Parameters that vary significantly with operating voltages or temperature are shown in the [Typical Characteristics](#) graphs.

8.4 Device Functional Modes

The μ A741 is powered on when the supply is connected. It can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

8.5 μ A741Y Chip Information

This chip, when properly assembled, displays characteristics similar to the μ A741C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The input offset voltage of operational amplifiers (op amps) arises from unavoidable mismatches in the differential input stage of the op-amp circuit caused by mismatched transistor pairs, collector currents, current-gain betas (β), collector or emitter resistors, etc. The input offset pins allow the designer to adjust for these mismatches by external circuitry. These input mismatches can be adjusted by putting resistors or a potentiometer between the inputs as shown in Figure 13. A potentiometer can be used to fine tune the circuit during testing or for applications which require precision offset control. More information about designing using the input-offset pins, see the application note *Nulling Input Offset Voltage of Operational Amplifiers*, [SLOA045](#).

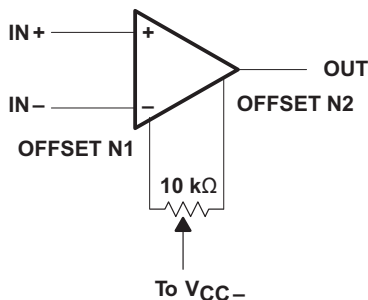


Figure 11. Input Offset Voltage Null Circuit

9.2 Typical Application

The voltage follower configuration of the operational amplifier is used for applications where a weak signal is used to drive a relatively high current load. This circuit is also called a buffer amplifier or unity gain amplifier. The inputs of an operational amplifier have a very high resistance which puts a negligible current load on the voltage source. The output resistance of the operational amplifier is almost negligible, so it can provide as much current as necessary to the output load.

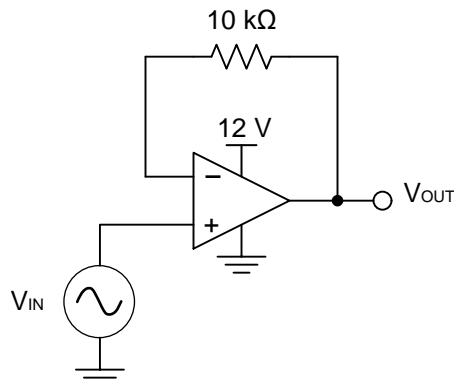


Figure 12. Voltage Follower Schematic

9.2.1 Design Requirements

- Output range of 2 V to 11.5 V
- Input range of 2 V to 11.5 V

Typical Application (continued)

- Resistive feedback to negative input

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Swing

The output voltage of an operational amplifier is limited by its internal circuitry to some level below the supply rails. For this amplifier, the output voltage swing is within ± 12 V, which accommodates the input and output voltage requirements.

9.2.2.2 Supply and Input Voltage

For correct operation of the amplifier, neither input must be higher than the recommended positive supply rail voltage or lower than the recommended negative supply rail voltage. The chosen amplifier must be able to operate at the supply voltage that accommodates the inputs. Because the input for this application goes up to 11.5 V, the supply voltage must be 12 V. Using a negative voltage on the lower rail rather than ground allows the amplifier to maintain linearity for inputs below 2 V.

9.2.3 Application Curves for Output Characteristics

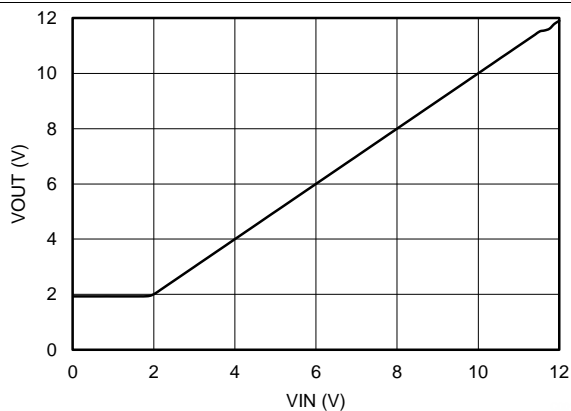


Figure 13. Output Voltage vs Input Voltage

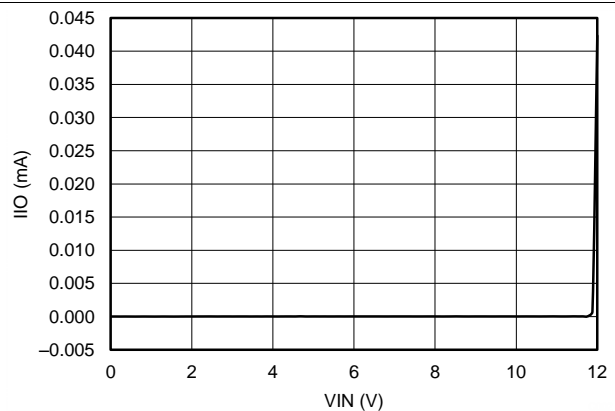


Figure 14. Current Drawn Input of Voltage Follower (I_{IO}) vs Input Voltage

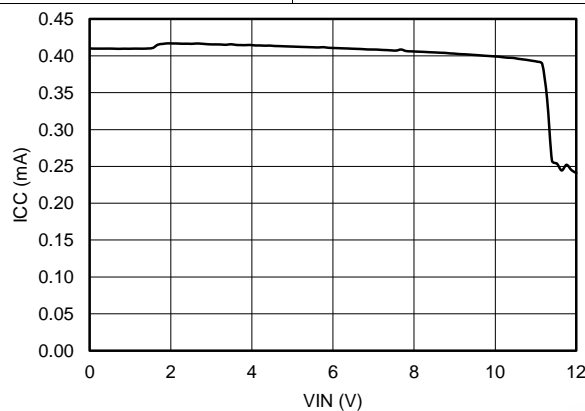


Figure 15. Current Drawn from Supply (I_{CC}) vs Input Voltage

10 Power Supply Recommendations

The μ A741 is specified for operation from ± 5 to ± 15 V; many specifications apply from 0°C to 70°C. The [Typical Characteristics](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than ± 18 V can permanently damage the device (see the [Absolute Maximum Ratings](#)).

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Layout Guidelines](#).

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to [Circuit Board Layout Techniques](#), [SLOA089](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Layout Example](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

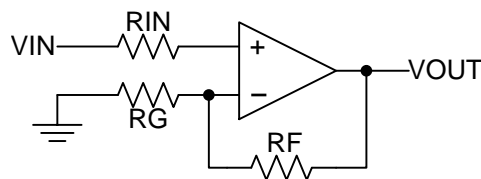


Figure 16. Operational Amplifier Schematic for Noninverting Configuration

Layout Example (continued)

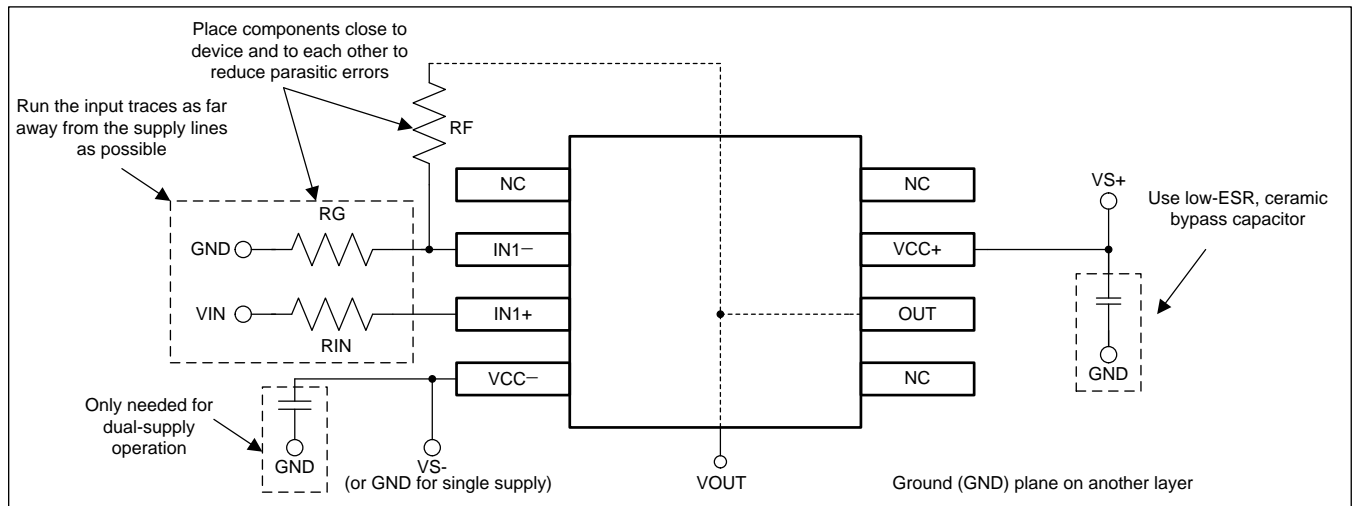


Figure 17. Operational Amplifier Board Layout for Noninverting Configuration

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA741CD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C	Samples
UA741CDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C	Samples
UA741CDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C	Samples
UA741CDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UA741C	Samples
UA741CJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	0 to 70		
UA741CJG4	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	0 to 70		
UA741CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UA741CP	Samples
UA741CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	UA741CP	Samples
UA741CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	U741	Samples
UA741CPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	U741	Samples
UA741MFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
UA741MJ	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
UA741MJB	OBSOLETE	CDIP	J	14		TBD	Call TI	Call TI	-55 to 125		
UA741MJG	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		
UA741MJGB	OBSOLETE	CDIP	JG	8		TBD	Call TI	Call TI	-55 to 125		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA741CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UA741CPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1

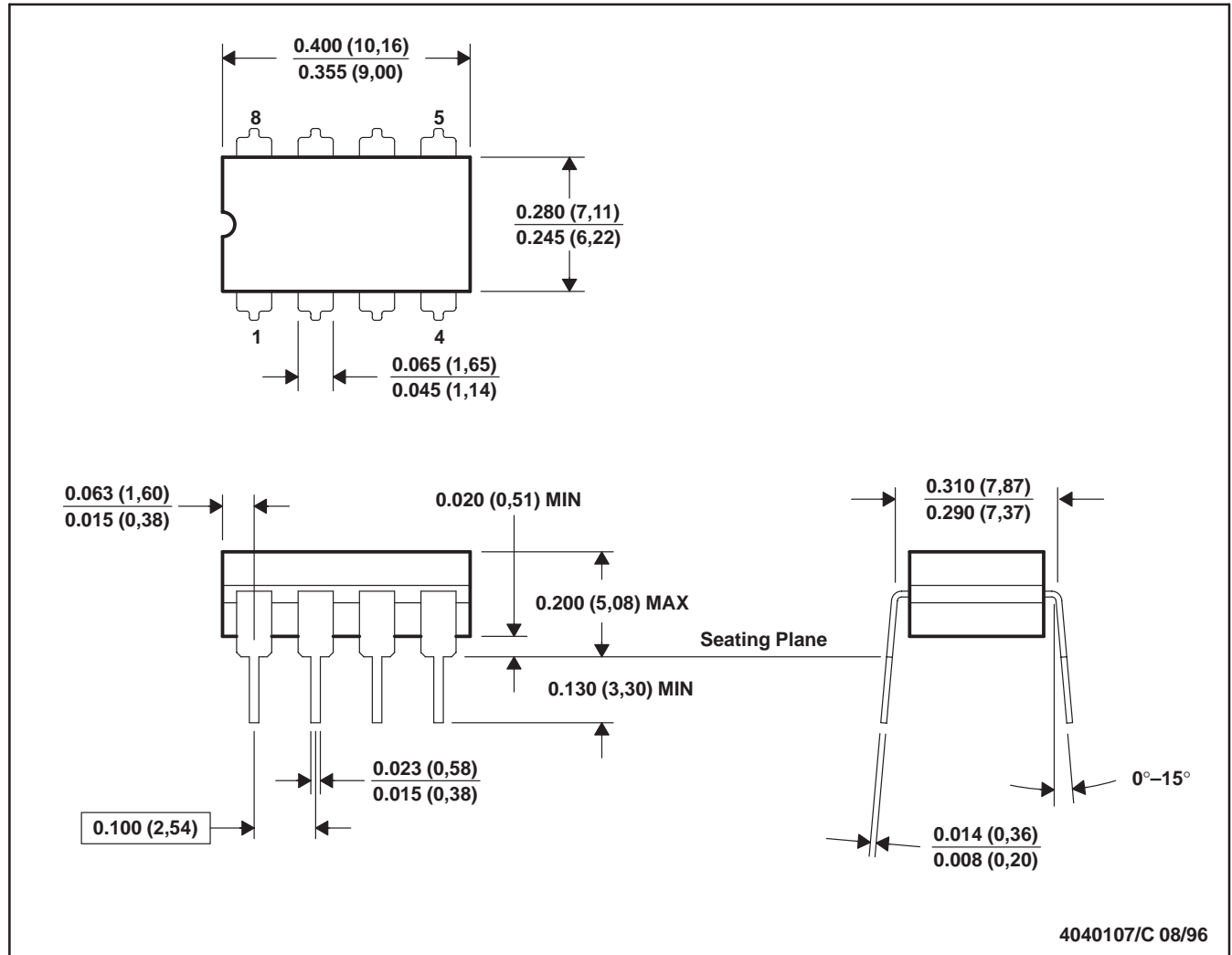
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA741CDR	SOIC	D	8	2500	340.5	338.1	20.6
UA741CPSR	SO	PS	8	2000	367.0	367.0	38.0

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



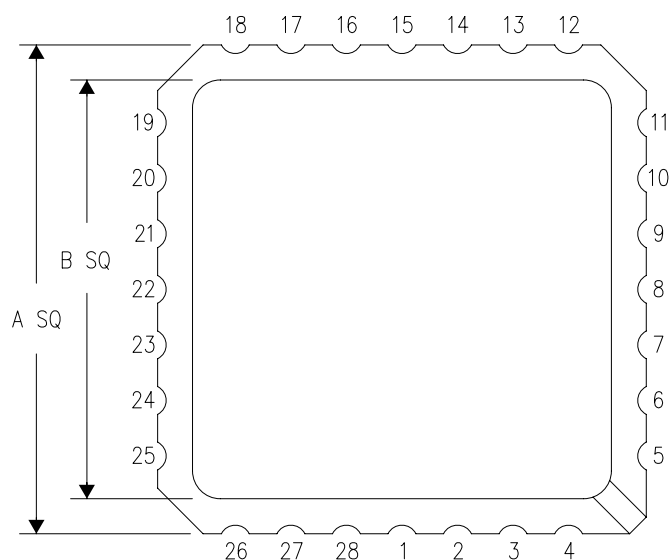
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

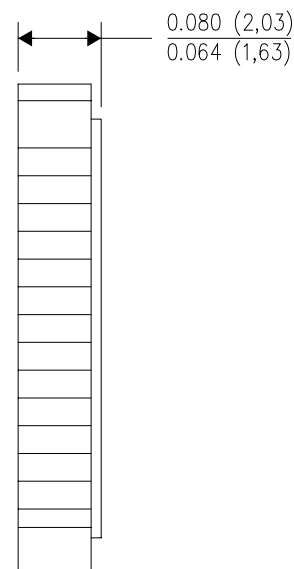
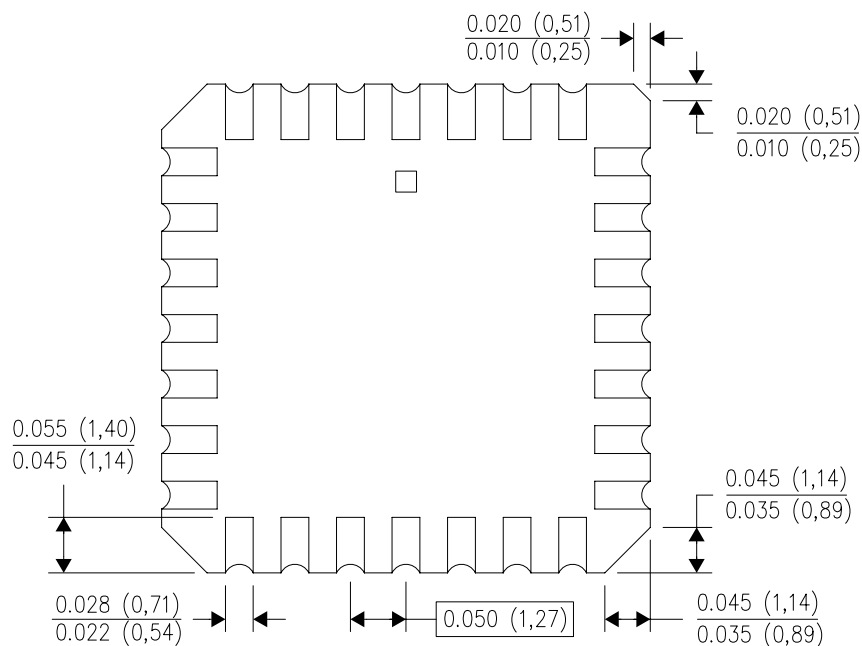
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

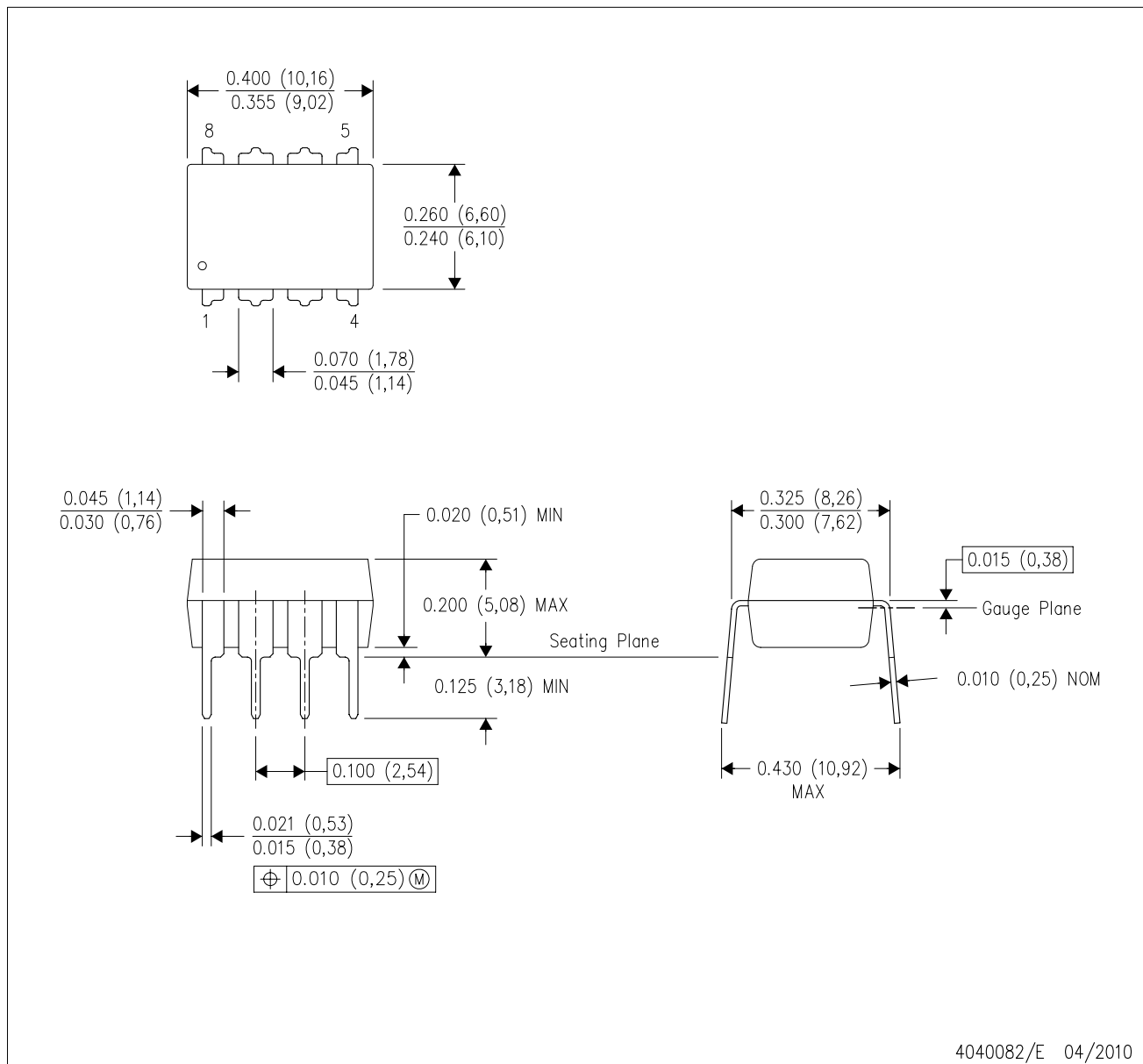


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

P (R-PDIP-T8)

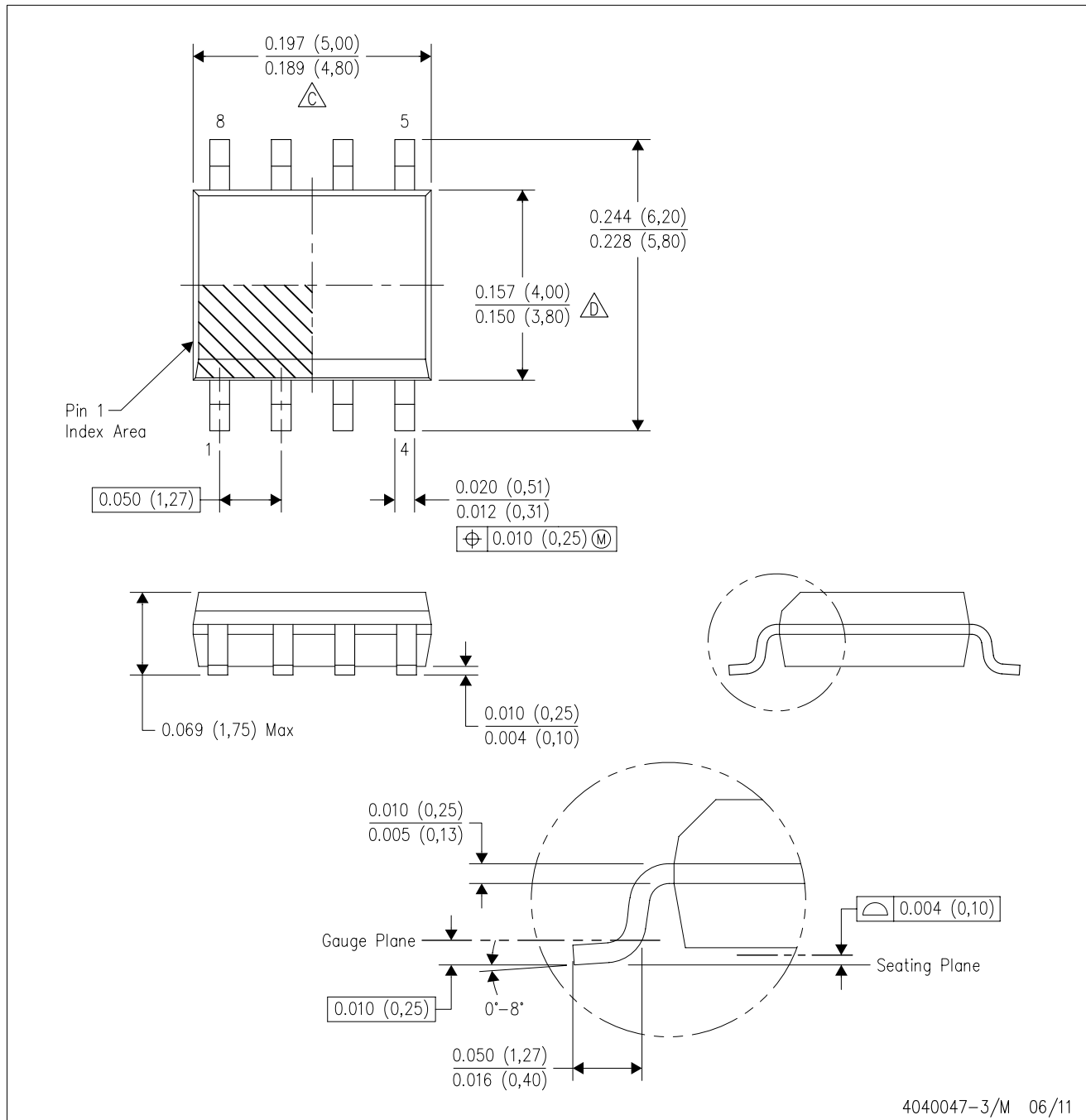
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

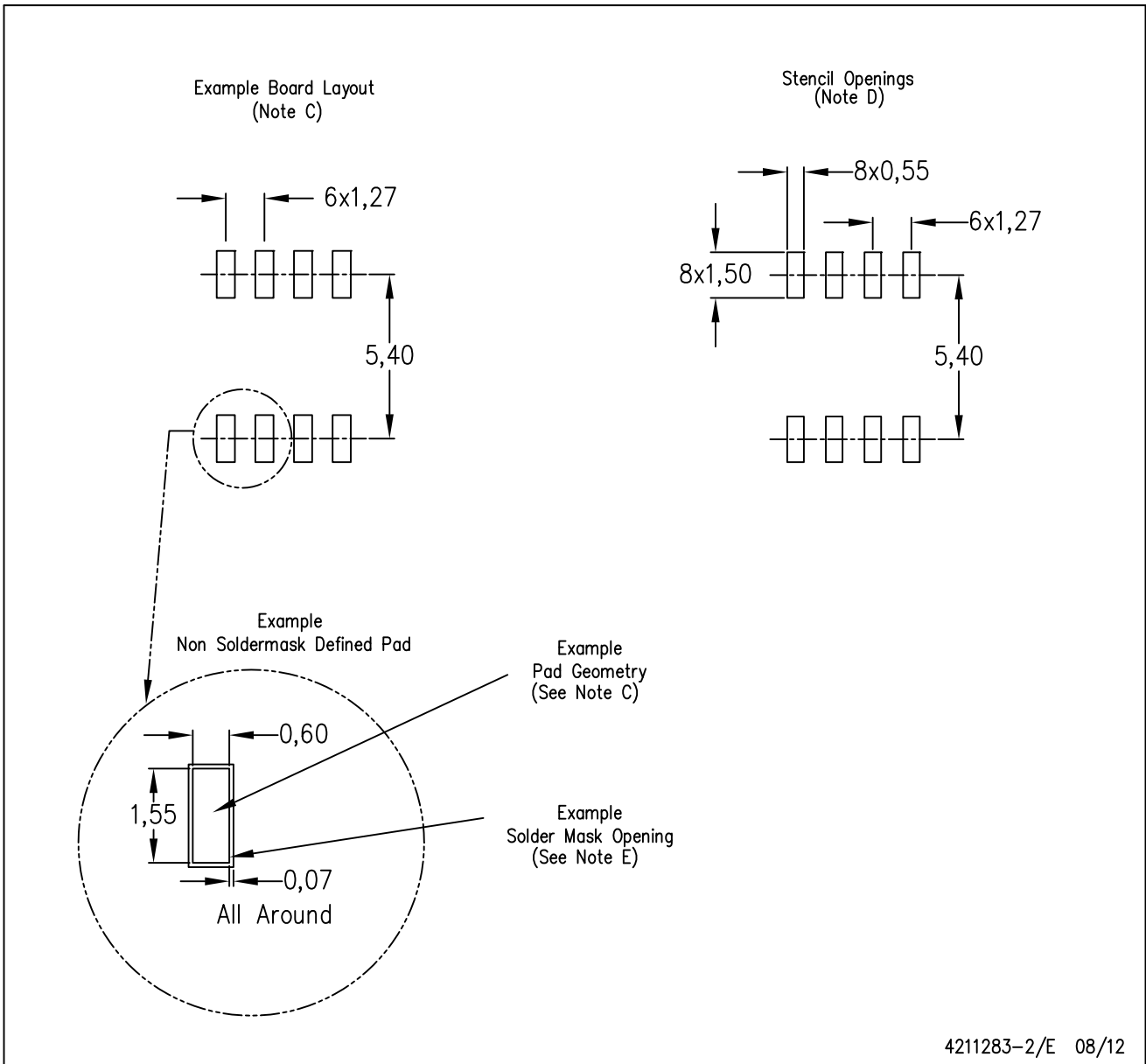
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

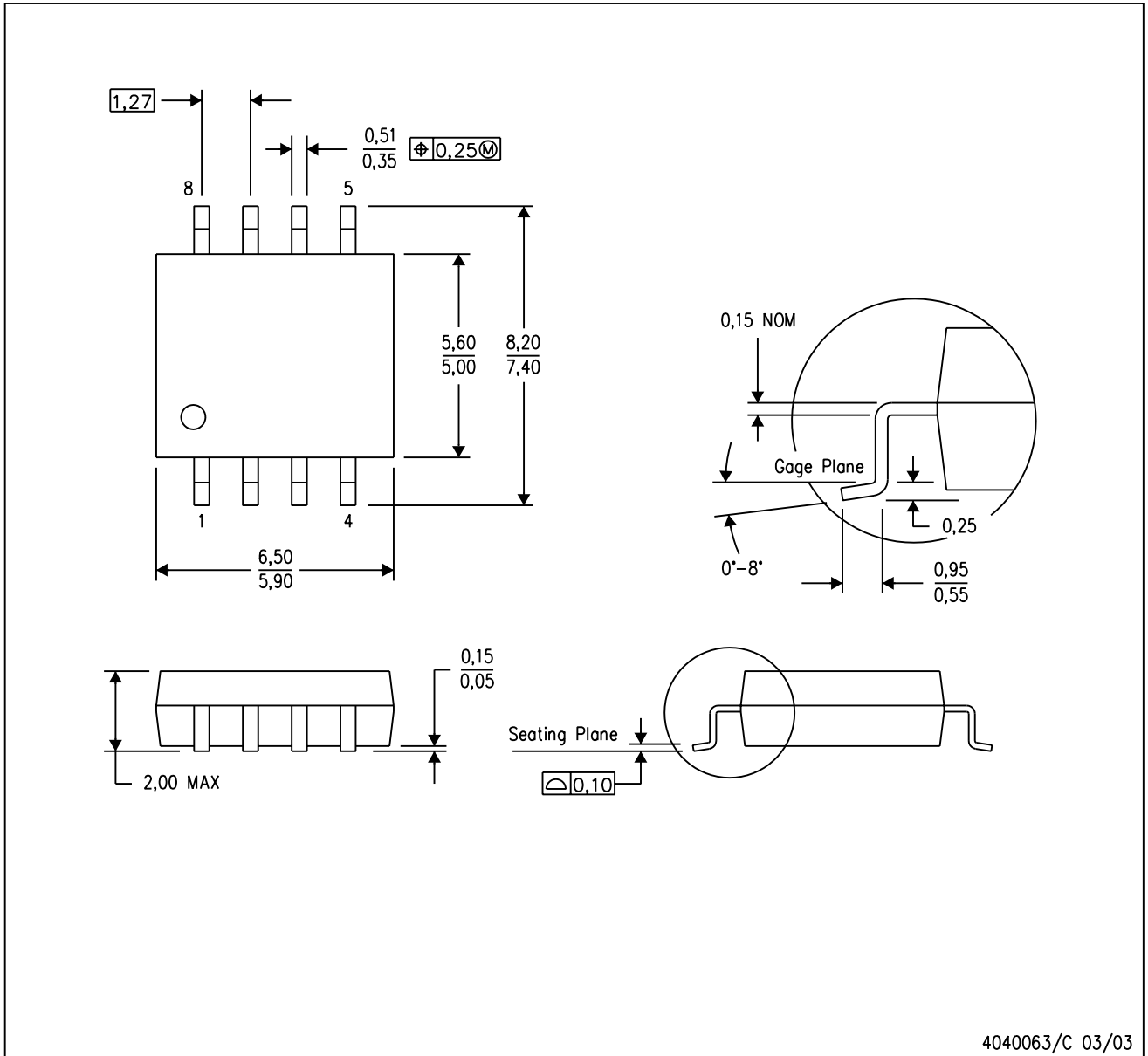


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PS (R-PDSO-G8)

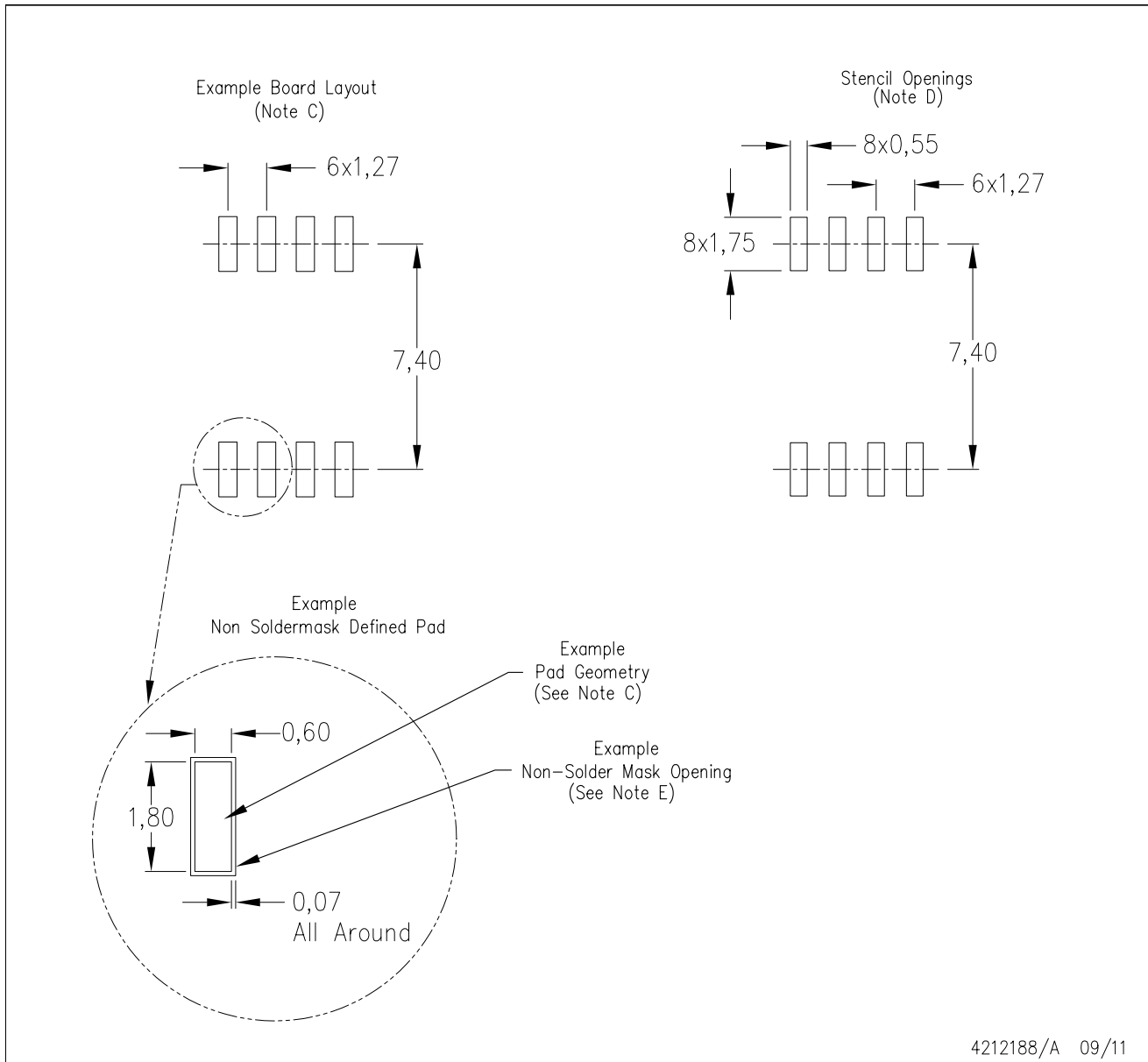
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com