



HESTORE.HU

elektronikai alkatrész áruház

EN: This Datasheet is presented by the manufacturer.

Please visit our website for pricing and availability at www.hestore.hu.

NCP5104, NCV5104

High Voltage, Half Bridge Driver

The NCP5104 is a High Voltage Power gate Driver providing two outputs for direct drive of 2 N-channel power MOSFETs or IGBTs arranged in a half-bridge configuration. It uses the bootstrap technique to insure a proper drive of the High-side power switch.

Features

- High Voltage Range: up to 600 V
- dV/dt Immunity ± 50 V/nsec
- Gate Drive Supply Range from 10 V to 20 V
- High and Low Drive Outputs
- Output Source / Sink Current Capability 250 mA / 500 mA
- 3.3 V and 5 V Input Logic Compatible
- Up to V_{CC} Swing on Input Pins
- Extended Allowable Negative Bridge Pin Voltage Swing to -10 V for Signal Propagation
- Matched Propagation Delays between Both Channels
- 1 Input with Internal Fixed Dead Time (520 ns)
- Under V_{CC} LockOut (UVLO) for Both Channels
- Pin to Pin Compatible with Industry Standards
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Half-Bridge Power Converters

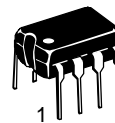


ON Semiconductor®

www.onsemi.com

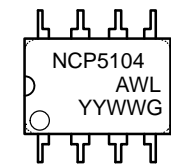
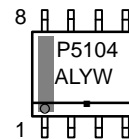


SOIC-8
D SUFFIX
CASE 751



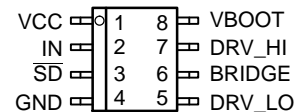
PDIP-8
P SUFFIX
CASE 626

MARKING DIAGRAMS



NCP5104 = Specific Device Code
 A = Assembly Location
 L or WL = Wafer Lot
 Y or YY = Year
 W or WW = Work Week
 G or ■ = Pb-Free Package

PINOUT INFORMATION



8 Pin Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP5104PG	PDIP-8 (Pb-Free)	50 Units / Rail
NCP5104DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
NCV5104DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCP5104, NCV5104

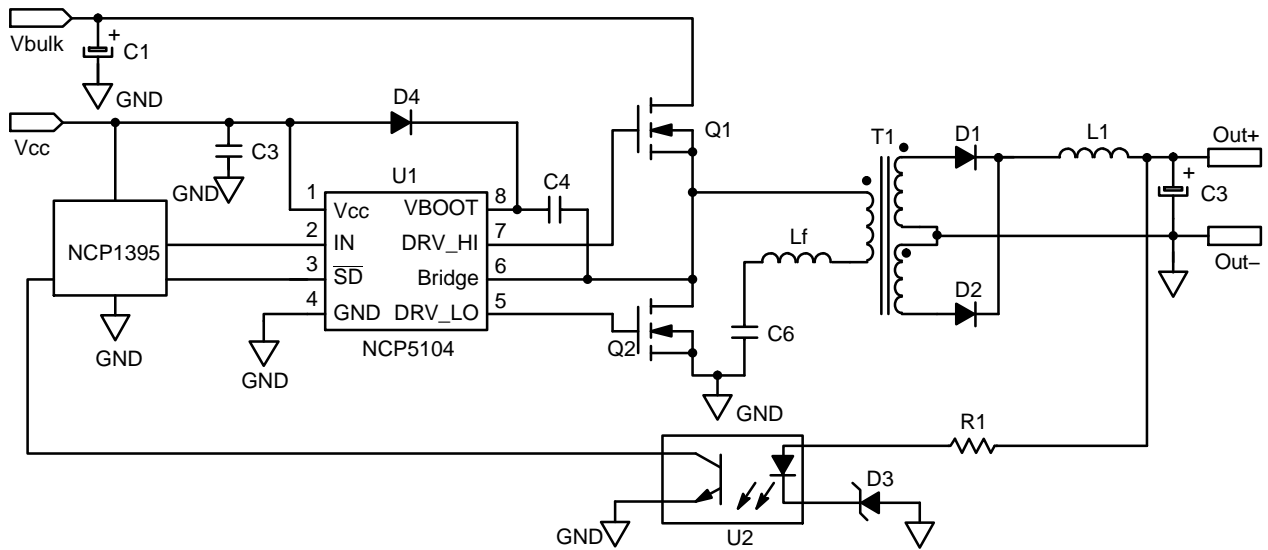


Figure 1. Typical Application Resonant Converter (LLC type)

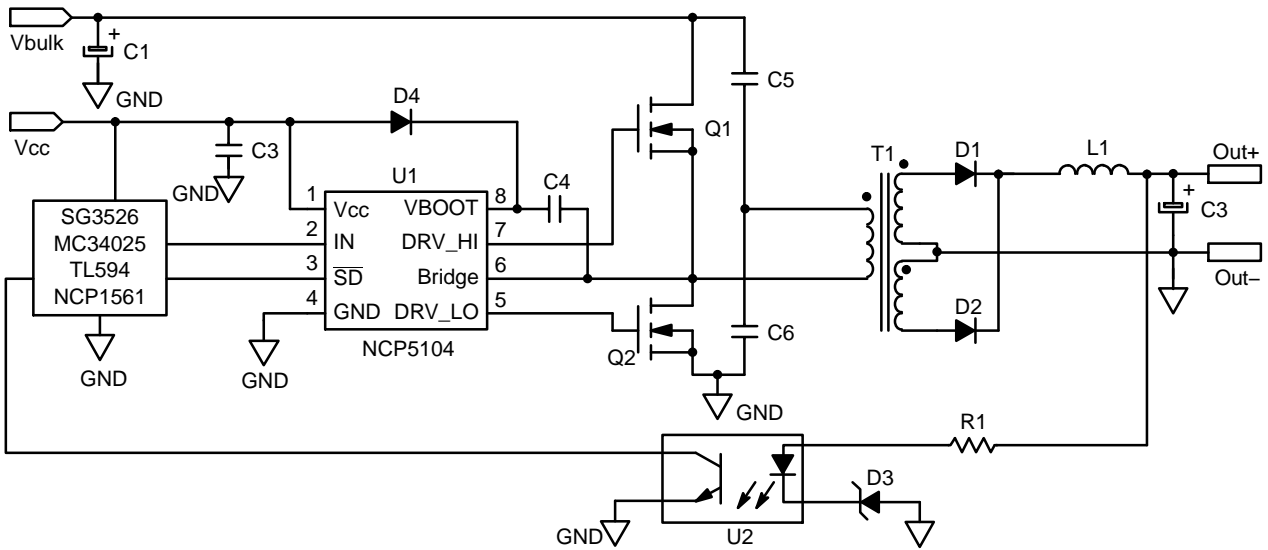


Figure 2. Typical Application Half Bridge Converter

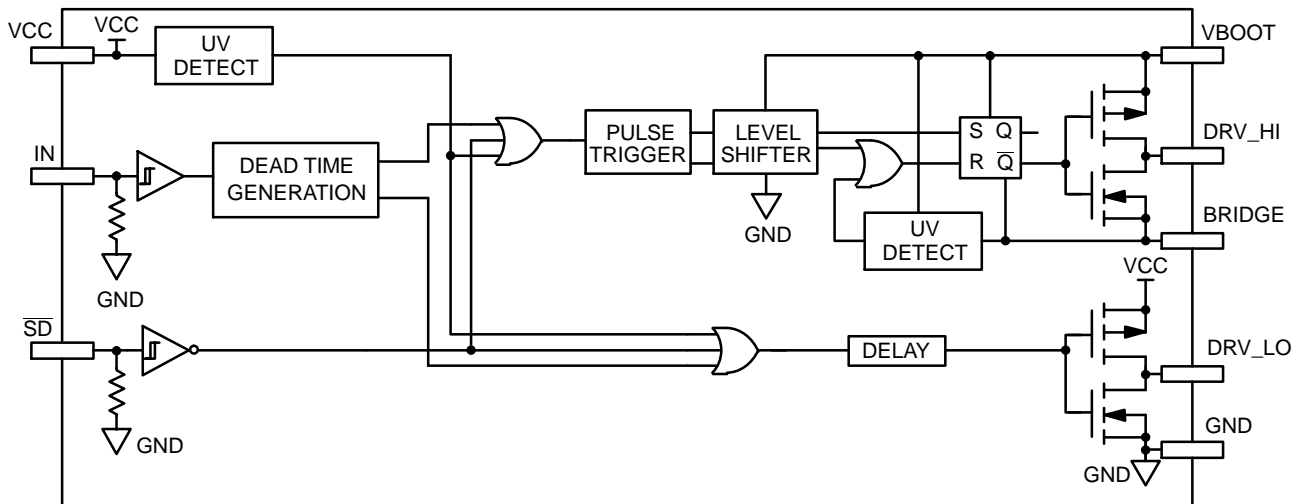


Figure 3. Detailed Block Diagram

NCP5104, NCV5104

PIN DESCRIPTION

Pin Name	Description
V _{CC}	Low Side and Main Power Supply
IN	Logic Input
\overline{SD}	Logic Input for Shutdown
GND	Ground
DRV_LO	Low Side Gate Drive Output
V _{BOOT}	Bootstrap Power Supply
DRV_HI	High Side Gate Drive Output
BRIDGE	Bootstrap Return or High Side Floating Supply Return

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V _{CC}	Main power supply voltage	-0.3 to 20	V
V _{CC_transient}	Main transient power supply voltage: I _{VCC_max} = 5 mA during 10 ms	23	V
V _{BOOT}	VHV: High Voltage BOOT Pin	-1 to 620	V
V _{BRIDGE}	VHV: High Voltage BRIDGE pin	-1 to 600	V
V _{BRIDGE}	Allowable Negative Bridge Pin Voltage for IN_LO Signal Propagation to DRV_LO (see characterization curves for detailed results)	-10	V
V _{BOOT-VBRIDGE}	VHV: Floating supply voltage	-0.3 to 20	V
V _{DRV_HI}	VHV: High side output voltage	V _{BRIDGE} - 0.3 to V _{BOOT} + 0.3	V
V _{DRV_LO}	Low side output voltage	-0.3 to V _{CC} + 0.3	V
dV _{BRIDGE} /dt	Allowable output slew rate	50	V/ns
V _{IN} , V _{SD}	Inputs IN & SD	-1.0 to V _{CC} + 0.3	V
	ESD Capability: – HBM model (all pins except pins 6–7–8 in 8) – Machine model (all pins except pins 6–7–8)	2 200	kV V
	Latch up capability per JEDEC JESD78		
R _{θJA}	Power dissipation and Thermal characteristics PDIP-8: Thermal Resistance, Junction-to-Air SO-8: Thermal Resistance, Junction-to-Air	100 178	°C/W
T _{ST}	Storage Temperature Range	-55 to +150	°C
T _{J_max}	Maximum Operating Junction Temperature	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NCP5104, NCV5104

ELECTRICAL CHARACTERISTIC ($V_{CC} = V_{boot} = 15\text{ V}$, $V_{GND} = V_{bridge}$, $-40^{\circ}\text{C} < T_J < 125^{\circ}\text{C}$, Outputs loaded with 1 nF)

Rating	Symbol	$T_J -40^{\circ}\text{C to } 125^{\circ}\text{C}$			Units
		Min	Typ	Max	

OUTPUT SECTION

Output high short circuit pulsed current $V_{DRV} = 0\text{ V}$, $PW \leq 10\ \mu\text{s}$ (Note 1)	$I_{DRVsource}$	–	250	–	mA
Output low short circuit pulsed current $V_{DRV} = V_{CC}$, $PW \leq 10\ \mu\text{s}$ (Note 1)	$I_{DRVsink}$	–	500	–	mA
Output resistor (Typical value @ 25°C) Source	R_{OH}	–	30	60	Ω
Output resistor (Typical value @ 25°C) Sink	R_{OL}	–	10	20	Ω
High level output voltage, $V_{BIAS} - V_{DRV_XX}$ @ $I_{DRV_XX} = 20\text{ mA}$	V_{DRV_H}	–	0.7	1.6	V
Low level output voltage V_{DRV_XX} @ $I_{DRV_XX} = 20\text{ mA}$	V_{DRV_L}	–	0.2	0.6	V

DYNAMIC OUTPUT SECTION

Turn-on propagation delay ($V_{bridge} = 0\text{ V}$) (Note 2)	t_{ON}	–	620	800	ns
Turn-off propagation delay ($V_{bridge} = 0\text{ V}$ or 50 V) (Note 3)	t_{OFF}	–	100	170	ns
Shutdown propagation delay, when Shutdown is enabled	t_{sd_en}	–	100	170	ns
Shutdown propagation delay, when Shutdown is disabled	t_{sd_dis}	–	620	800	ns
Output voltage rise time (from 10% to 90% @ $V_{CC} = 15\text{ V}$) with 1 nF load	t_r	–	85	160	ns
Output voltage fall time (from 90% to 10% @ $V_{CC} = 15\text{ V}$) with 1 nF load	t_f	–	35	75	ns
Propagation delay matching between the High side and the Low side @ 25°C (Note 4)	Δt	–	10	45	ns
Internal fixed dead time (Note 5)	DT	400	520	650	ns

INPUT SECTION

Low level input voltage threshold	V_{IN}	–	–	0.8	V
Input pull-down resistor ($V_{IN} < 0.5\text{ V}$)	R_{IN}	–	200	–	k Ω
High level input voltage threshold	V_{IN}	2.3	–	–	V
Logic “1” input bias current @ $V_{IN} = 5\text{ V}$ @ 25°C	I_{IN+}	–	5	25	μA
Logic “0” input bias current @ $V_{IN} = 0\text{ V}$ @ 25°C	I_{IN-}	–	–	2.0	μA

SUPPLY SECTION

Vcc UV Start-up voltage threshold	V_{cc_stup}	8.0	8.9	9.8	V
Vcc UV Shut-down voltage threshold	V_{cc_shtdwn}	7.3	8.2	9.0	V
Hysteresis on Vcc	V_{cc_hyst}	0.3	0.7	–	V
Vboot Start-up voltage threshold reference to bridge pin ($V_{boot_stup} = V_{boot} - V_{bridge}$)	V_{boot_stup}	8.0	8.9	9.8	V
Vboot UV Shut-down voltage threshold	V_{boot_shtdwn}	7.3	8.2	9.0	V
Hysteresis on Vboot	V_{boot_shtdwn}	0.3	0.7	–	V
Leakage current on high voltage pins to GND ($V_{BOOT} = V_{BRIDGE} = DRV_HI = 600\text{ V}$)	I_{HV_LEAK}	–	5	40	μA
Consumption in active mode ($V_{cc} = V_{boot}$, $f_{sw} = 100\text{ kHz}$ and 1 nF load on both driver outputs)	ICC1	–	4	5	mA
Consumption in inhibition mode ($V_{cc} = V_{boot}$)	ICC2	–	250	400	μA
Vcc current consumption in inhibition mode	ICC3	–	200	–	μA
Vboot current consumption in inhibition mode	ICC4	–	50	–	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Parameter guaranteed by design.
2. $T_{ON} = T_{OFF} + DT$
3. Turn-off propagation delay @ $V_{bridge} = 600\text{ V}$ is guaranteed by design.
4. See characterization curve for Δt parameters variation on the full range temperature.
5. Timing diagram definition see: Figure 4, Figure 5 and Figure 6.

NCP5104, NCV5104

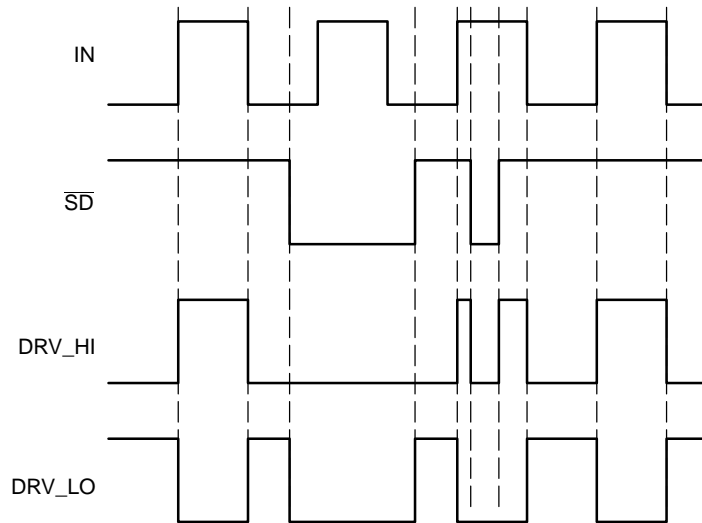


Figure 4. Input/Output Timing Diagram

Note: DRV_HI output is in phase with the input

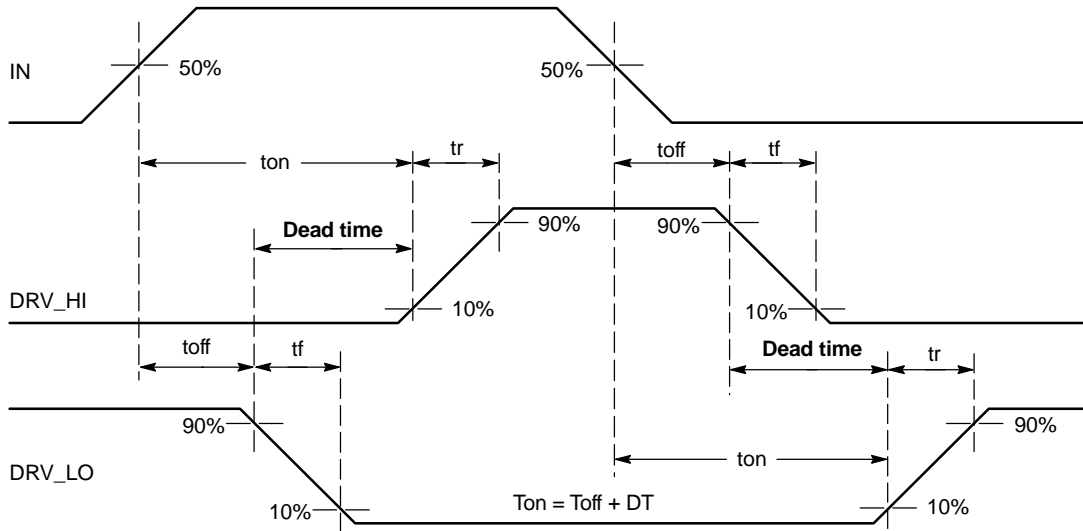


Figure 5. Timing Definitions

NCP5104, NCV5104

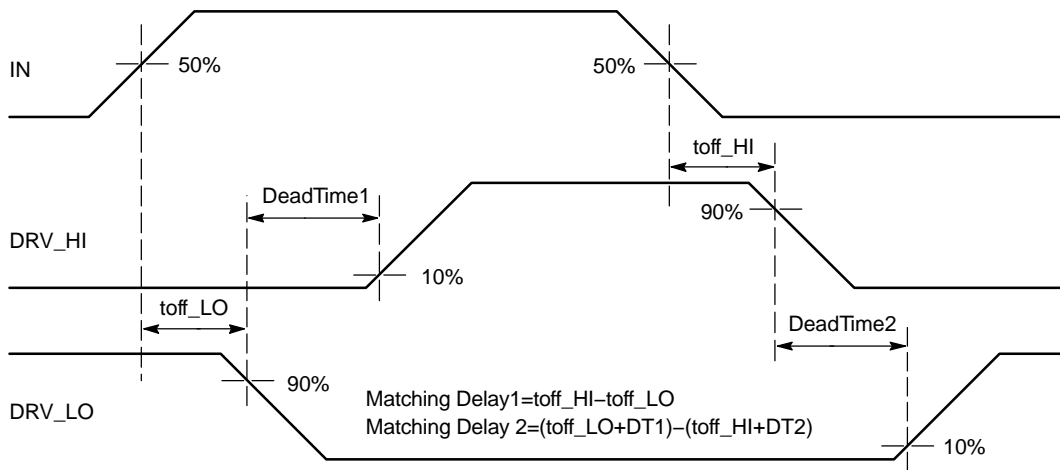


Figure 6. Matching Propagation Delay Definition

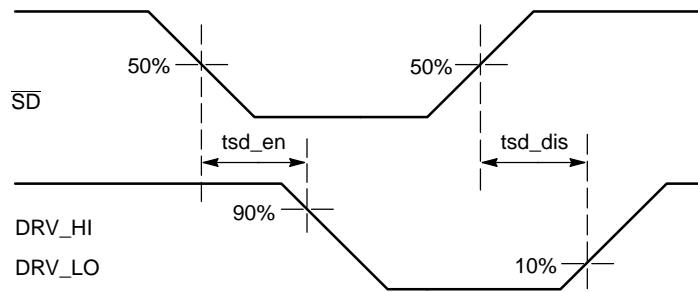


Figure 7. Shutdown Waveform Definition

NCP5104, NCV5104

CHARACTERIZATION CURVES

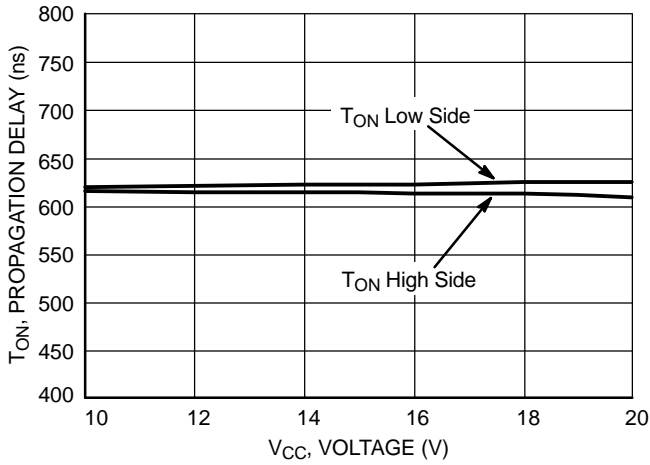


Figure 8. Turn ON Propagation Delay vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

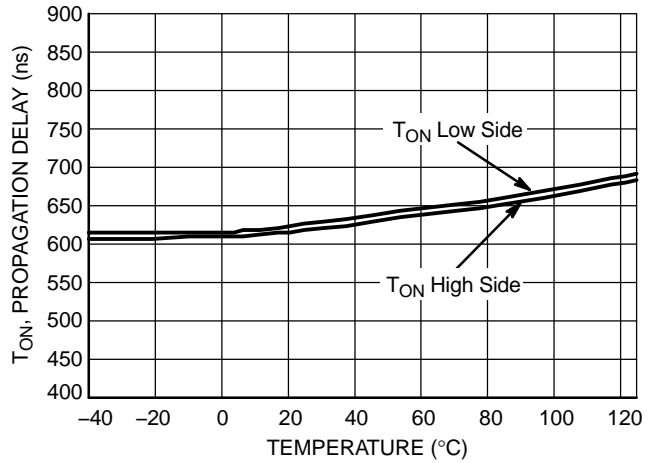


Figure 9. Turn ON Propagation Delay vs. Temperature

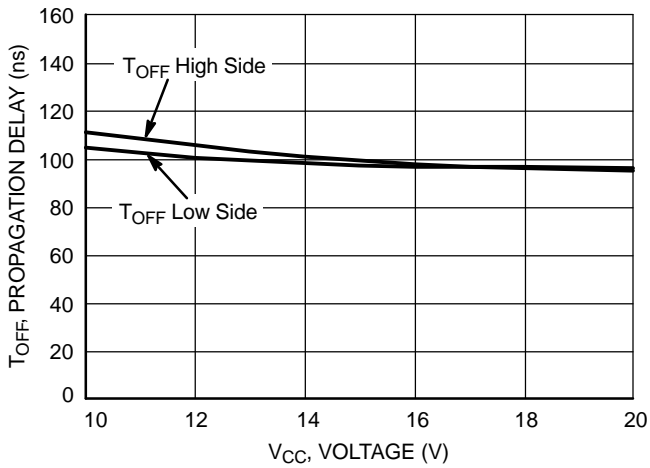


Figure 10. Turn OFF Propagation Delay vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

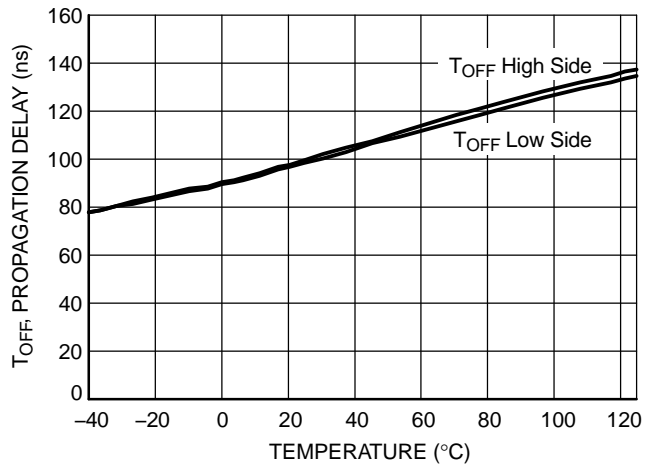


Figure 11. Turn OFF Propagation Delay vs. Temperature

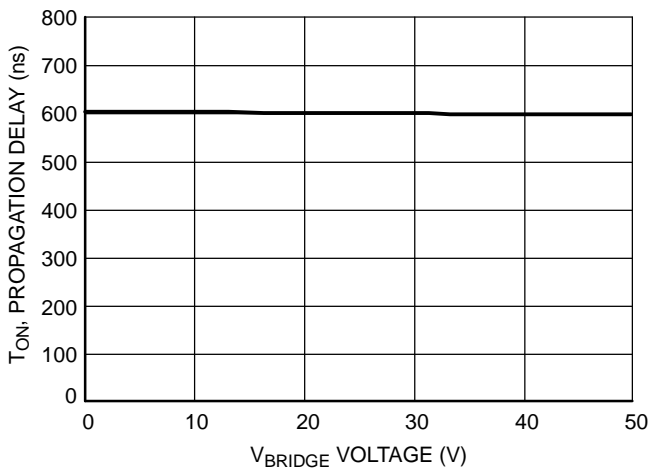


Figure 12. High Side Turn ON Propagation Delay vs. V_{BRIDGE} Voltage ($V_{CC} = V_{BOOT}$)

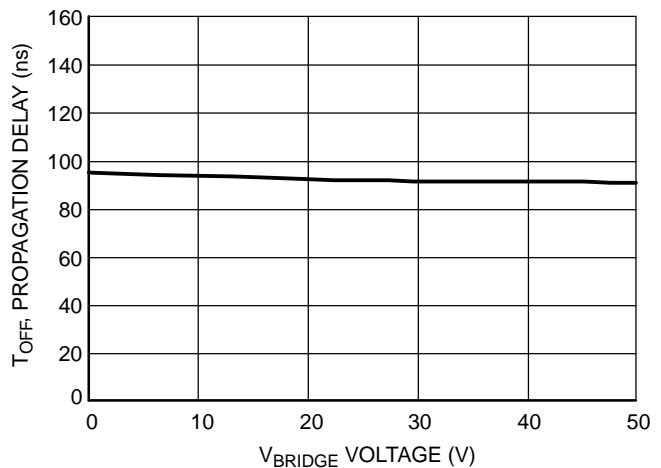


Figure 13. High Side Turn OFF Propagation Delay vs. V_{BRIDGE} Voltage ($V_{CC} = V_{BOOT}$)

NCP5104, NCV5104

CHARACTERIZATION CURVES

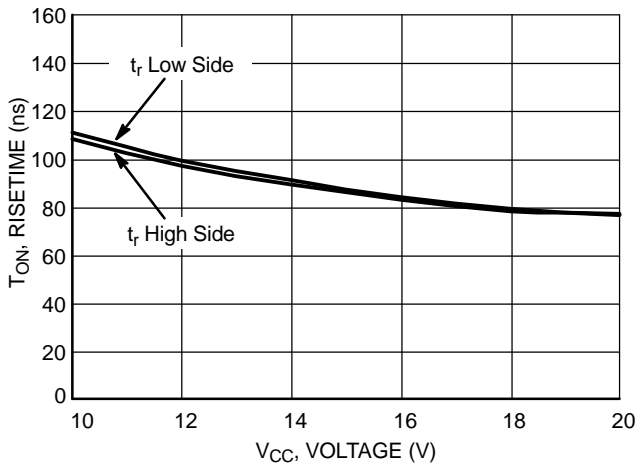


Figure 14. Turn ON Risetime vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

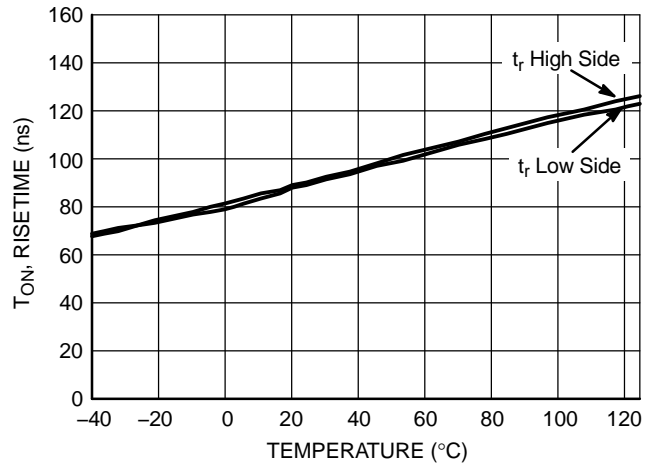


Figure 15. Turn ON Risetime vs. Temperature

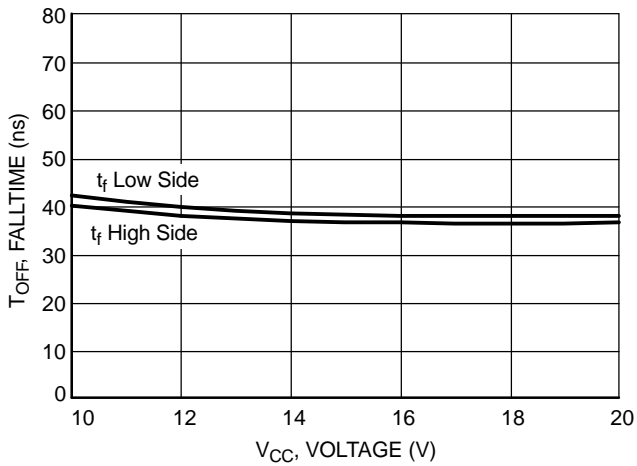


Figure 16. Turn OFF Falltime vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

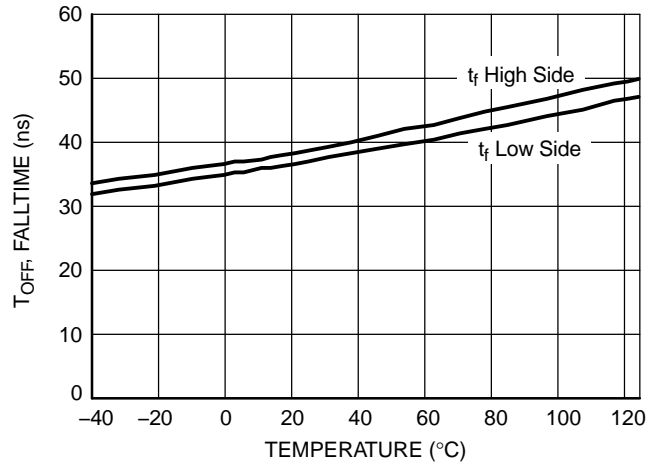


Figure 17. Turn OFF Falltime vs. Temperature

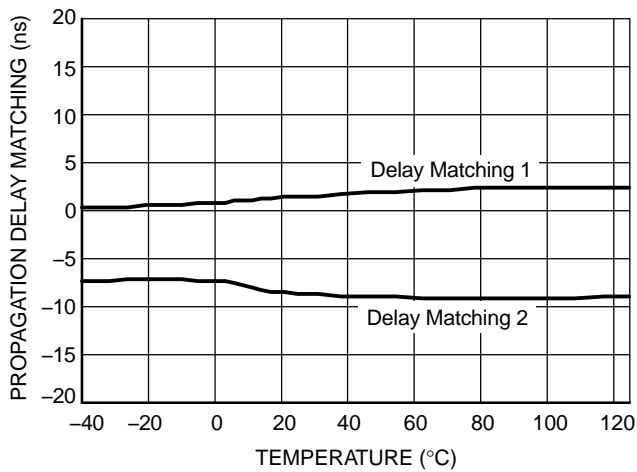


Figure 18. Propagation Delay Matching Between High Side and Low Side Driver vs. Temperature

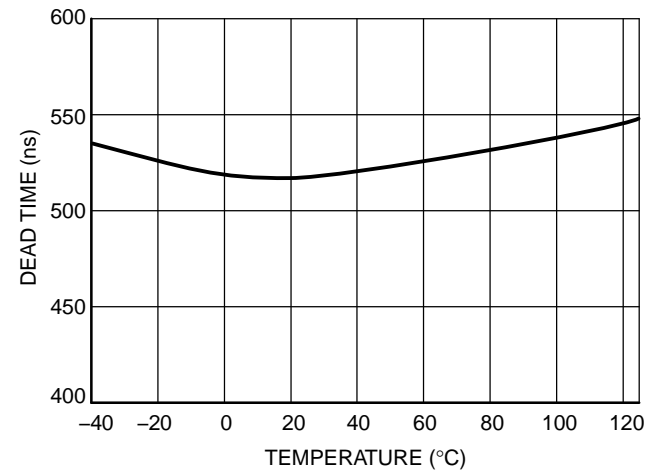


Figure 19. Dead Time vs. Temperature

CHARACTERIZATION CURVES

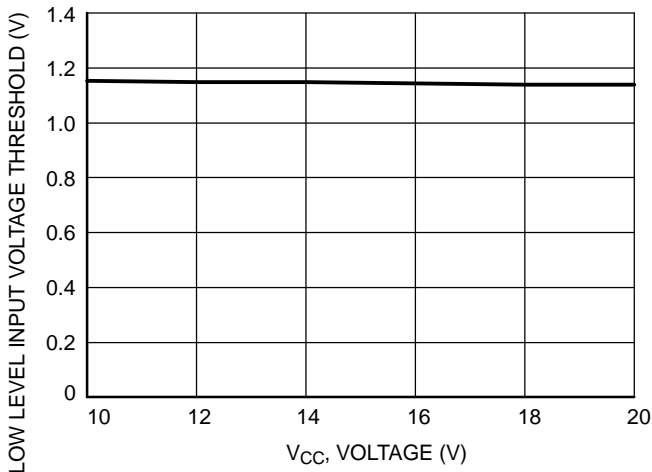


Figure 20. Low Level Input Voltage Threshold vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

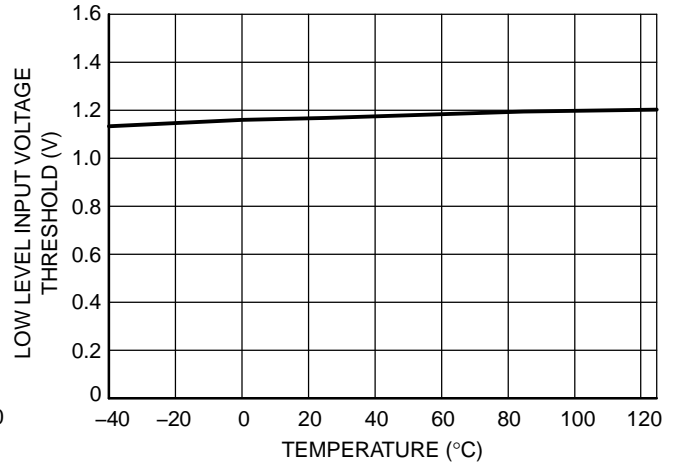


Figure 21. Low Level Input Voltage Threshold vs. Temperature

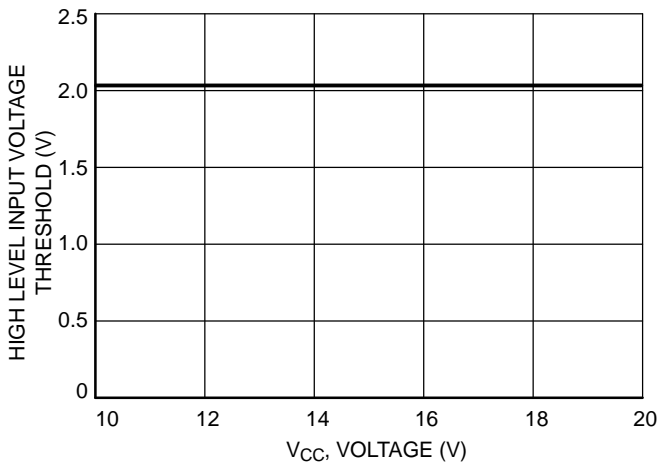


Figure 22. High Level Input Voltage Threshold vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

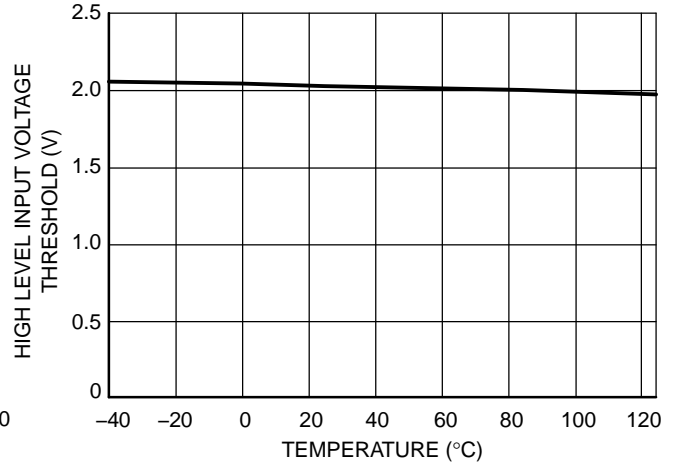


Figure 23. High Level Input Voltage Threshold vs. Temperature

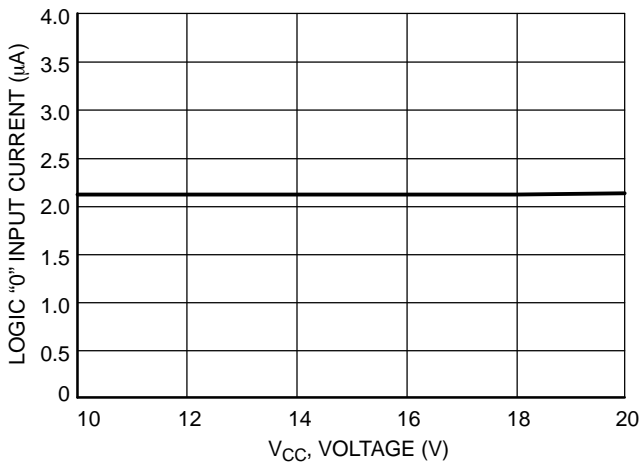


Figure 24. Logic "0" Input Current vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

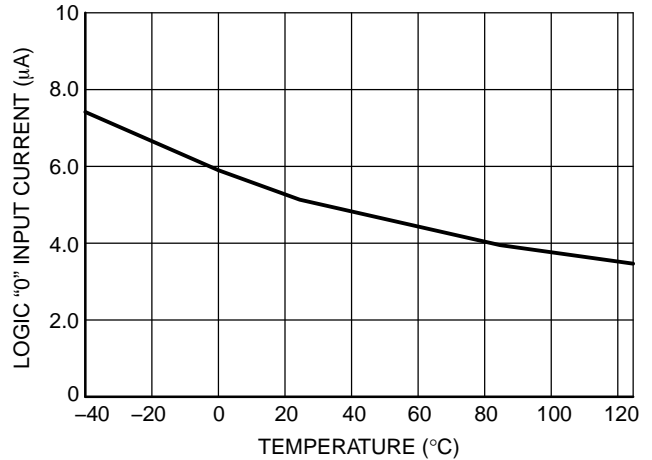


Figure 25. Logic "0" Input Current vs. Temperature

NCP5104, NCV5104

CHARACTERIZATION CURVES

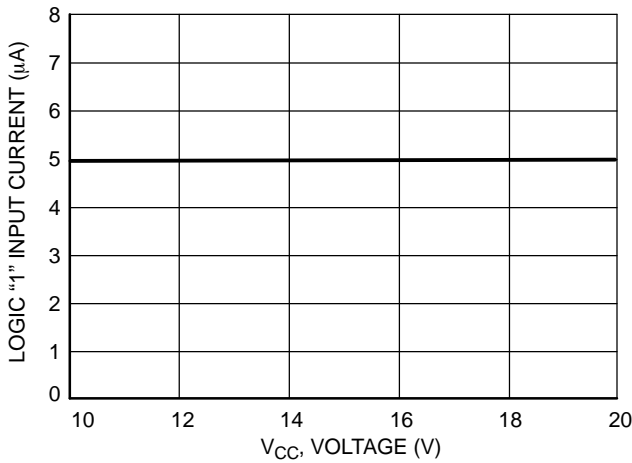


Figure 26. Logic "1" Input Current vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

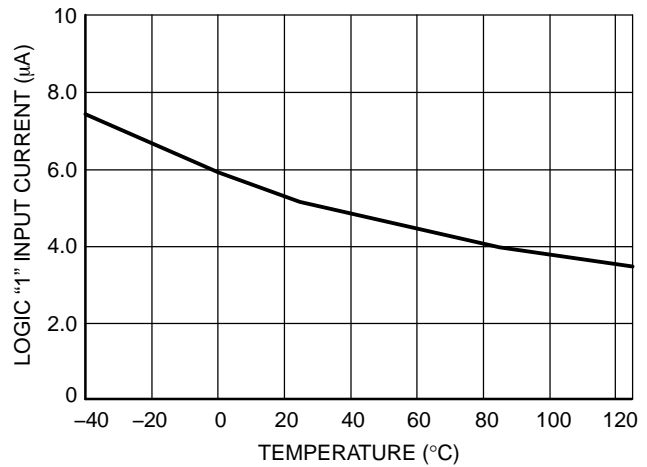


Figure 27. Logic "1" Input Current vs. Temperature

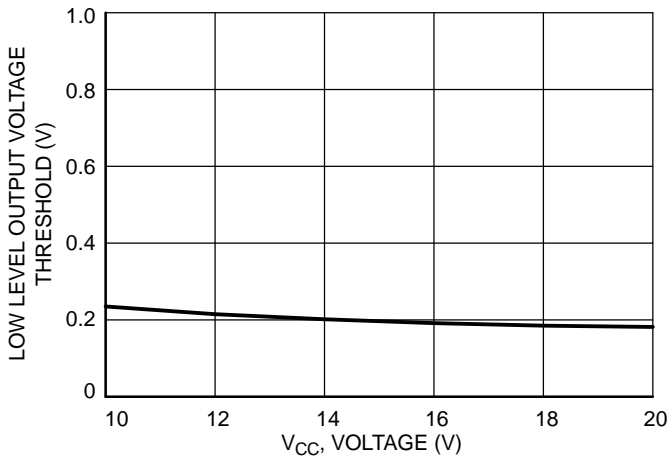


Figure 28. Low Level Output Voltage vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

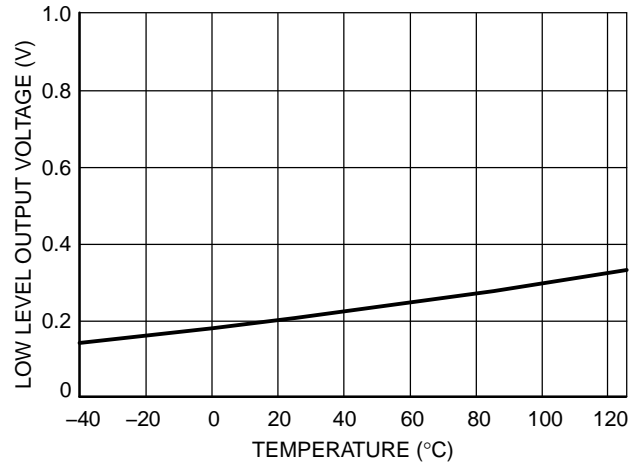


Figure 29. Low Level Output Voltage vs. Temperature

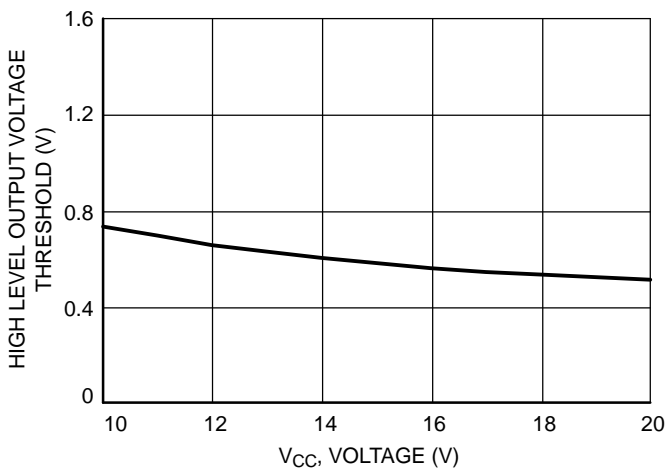


Figure 30. High Level Output Voltage vs. Supply Voltage ($V_{CC} = V_{BOOT}$)

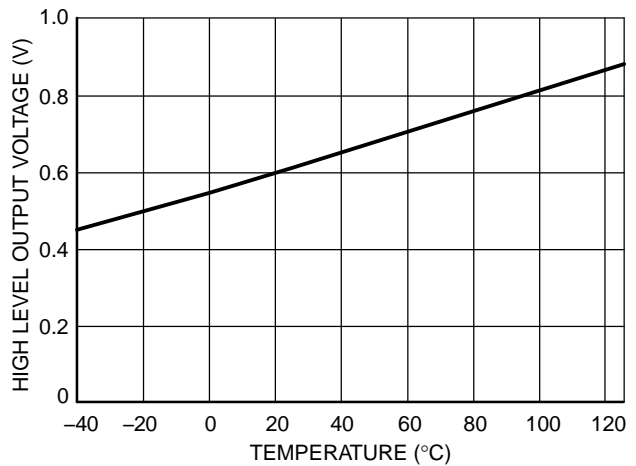


Figure 31. High Level Output Voltage vs. Temperature

NCP5104, NCV5104

CHARACTERIZATION CURVES

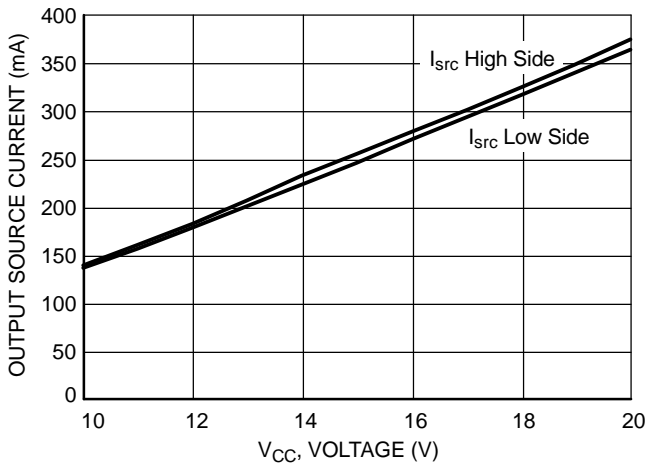


Figure 32. Output Source Current vs. Supply Voltage (V_{CC} = V_{BOOT})

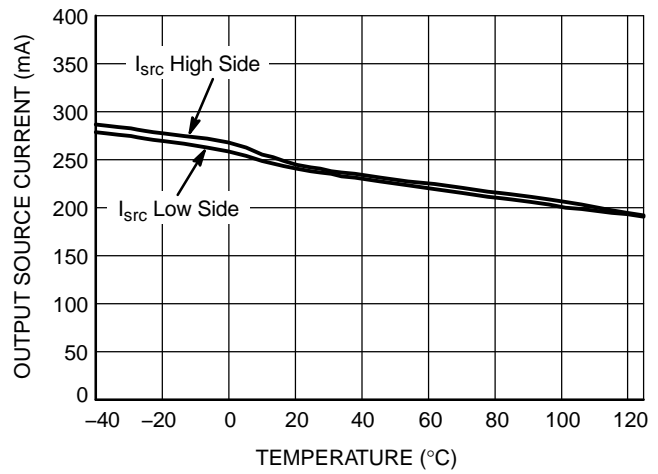


Figure 33. Output Source Current vs. Temperature

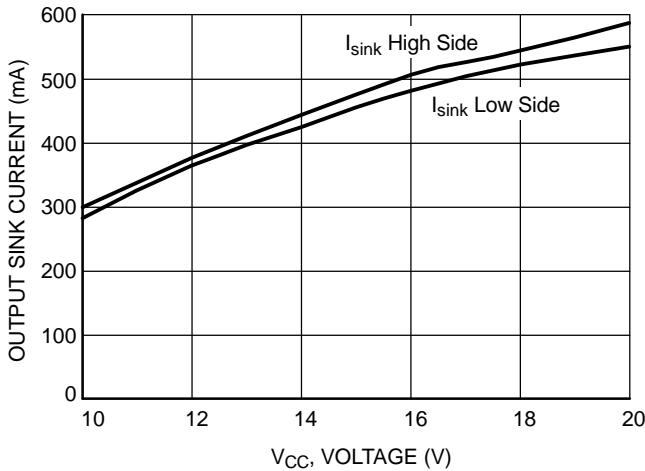


Figure 34. Output Sink Current vs. Supply Voltage (V_{CC} = V_{BOOT})

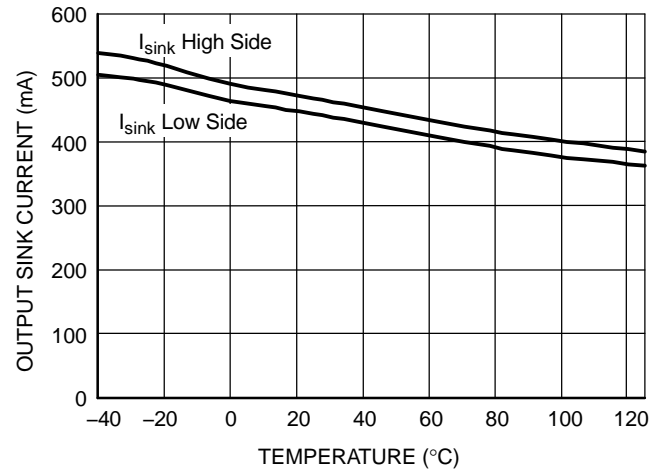


Figure 35. Output Sink Current vs. Temperature

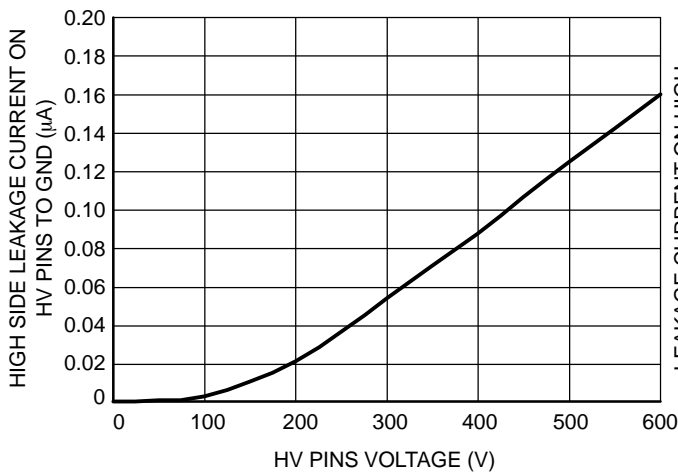


Figure 36. Leakage Current on High Voltage Pins (600 V) to Ground vs. V_{BRIDGE} Voltage (V_{BRIDGE} = V_{BOOT} = V_{DRV_HI})

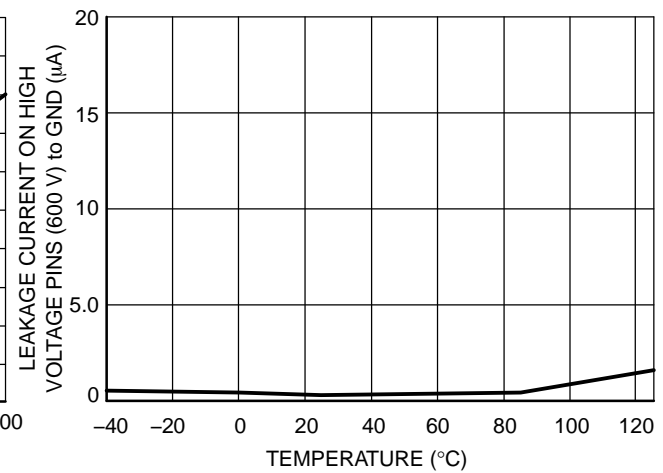


Figure 37. Leakage Current on High Voltage Pins (600 V) to Ground vs. Temperature (V_{BRIDGE} = V_{BOOT} = V_{DRV_HI} = 600 V)

CHARACTERIZATION CURVES

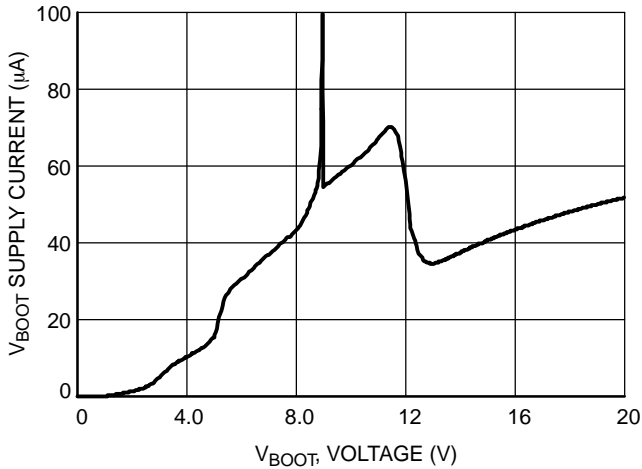


Figure 38. V_{BOOT} Supply Current vs. Bootstrap Supply Voltage ($V_{CC} = V_{BOOT}$)

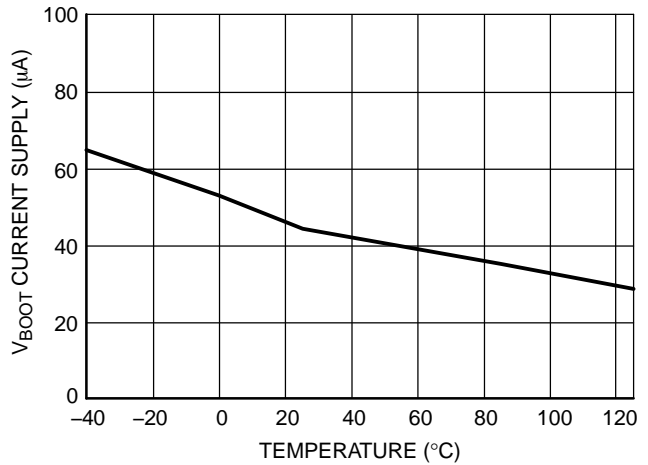


Figure 39. V_{BOOT} Supply Current vs. Temperature

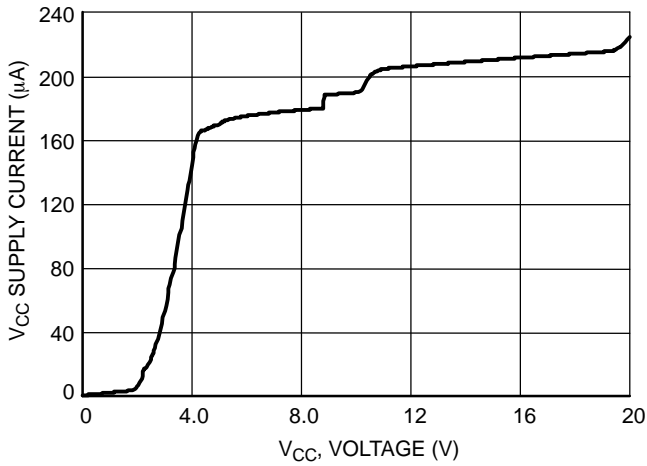


Figure 40. V_{CC} Supply Current vs. V_{CC} Supply Voltage ($V_{CC} = V_{BOOT}$)

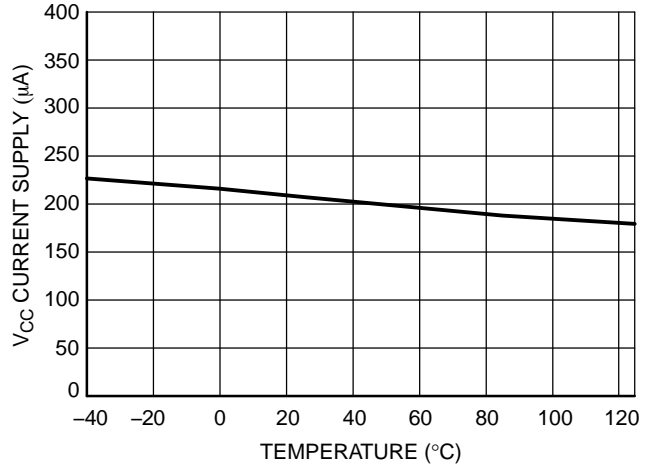


Figure 41. V_{CC} Supply Current vs. Temperature

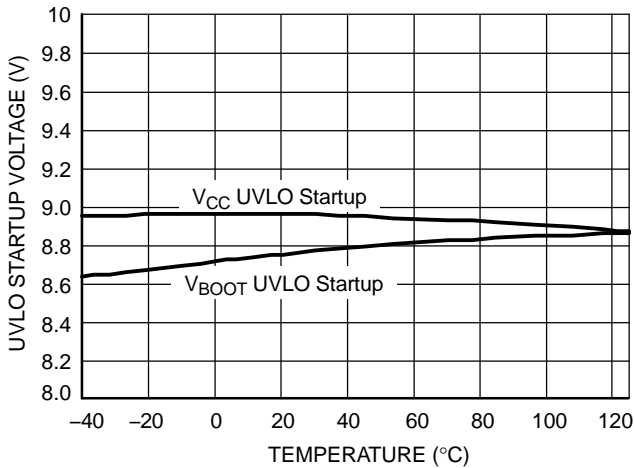


Figure 42. UVLO Startup Voltage vs. Temperature

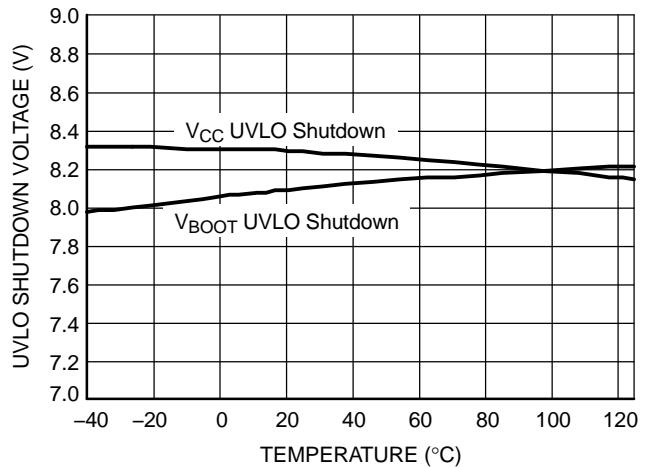


Figure 43. UVLO Shutdown Voltage vs. Temperature

CHARACTERIZATION CURVES

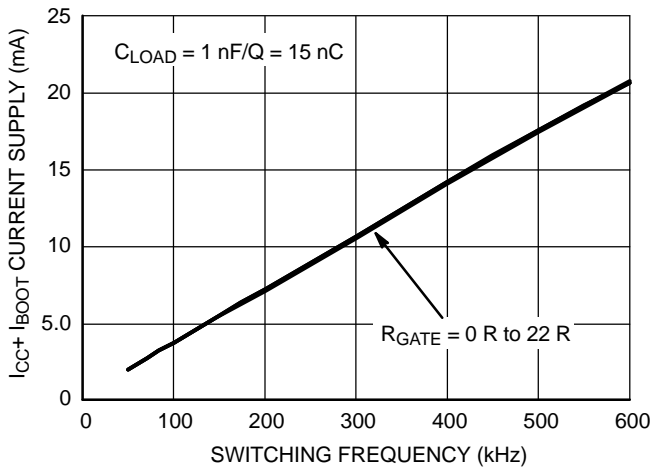


Figure 44. I_{CC1} Consumption vs. Switching Frequency with 15 nC Load on Each Driver @ $V_{CC} = 15 V$

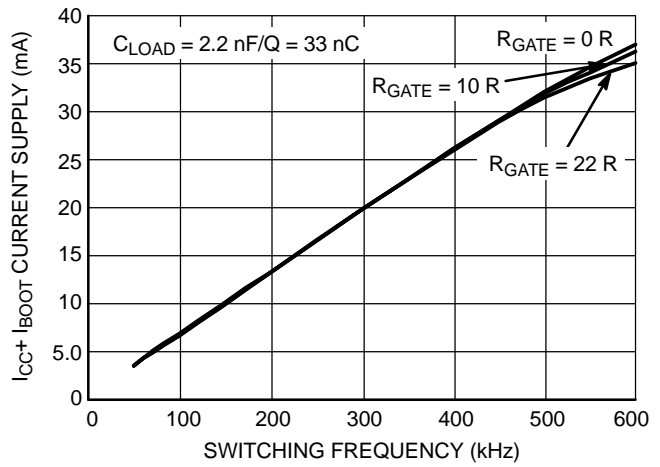


Figure 45. I_{CC1} Consumption vs. Switching Frequency with 33 nC Load on Each Driver @ $V_{CC} = 15 V$

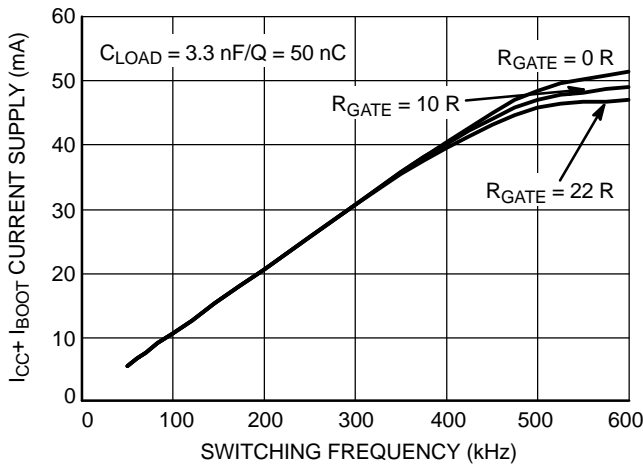


Figure 46. I_{CC1} Consumption vs. Switching Frequency with 50 nC Load on Each Driver @ $V_{CC} = 15 V$

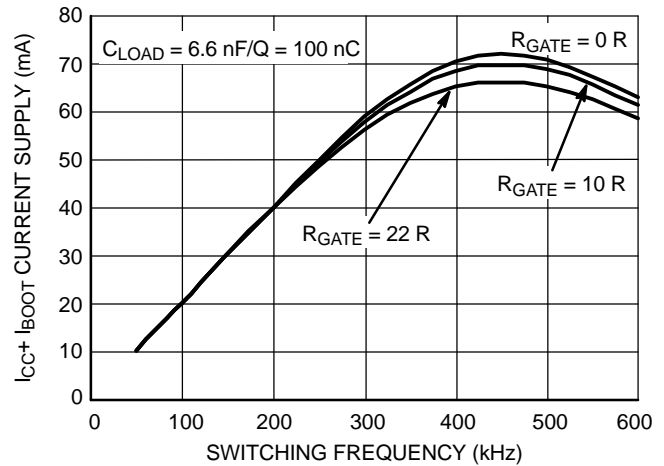


Figure 47. I_{CC1} Consumption vs. Switching Frequency with 100 nC Load on Each Driver @ $V_{CC} = 15 V$

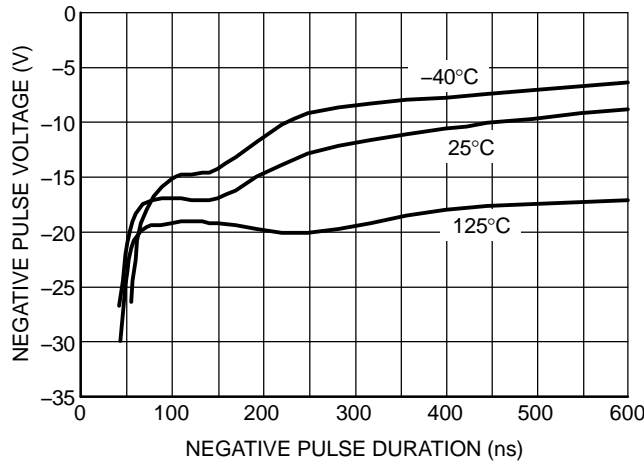
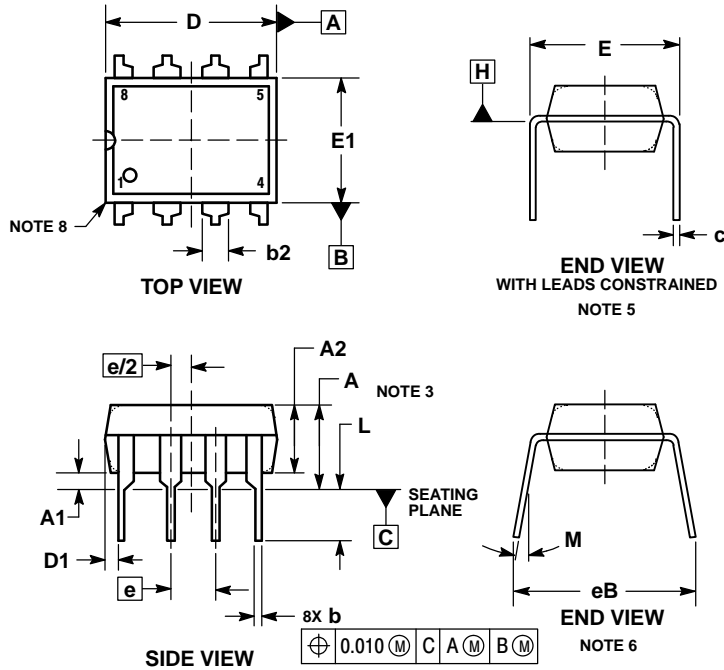


Figure 48. NCP5104, Negative Voltage Safe Operating Area on the Bridge Pin

NCP5104, NCV5104

PACKAGE DIMENSIONS

8 LEAD PDIP CASE 626-05 ISSUE N



NOTES:

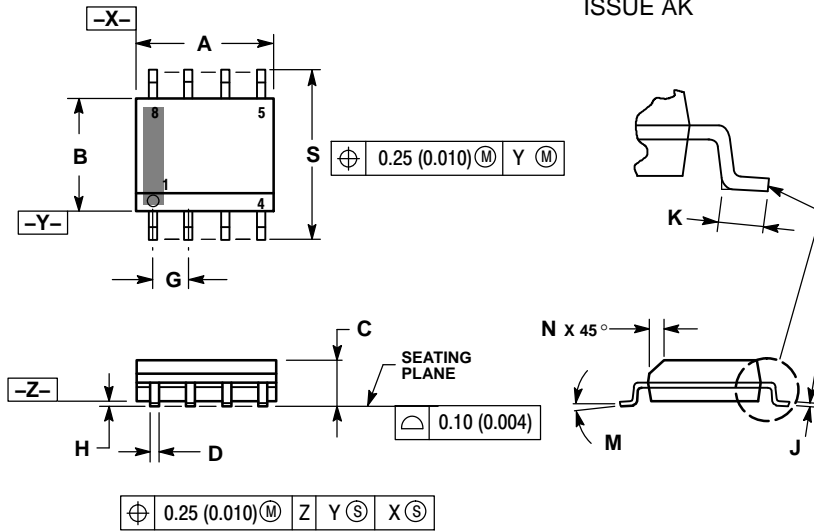
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS-3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION E3 IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	----	0.210	----	5.33
A1	0.015	----	0.38	----
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	----
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	----	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	----	10°

NCP5104, NCV5104

PACKAGE DIMENSIONS

SOIC-8 NB CASE 751-07 ISSUE AK

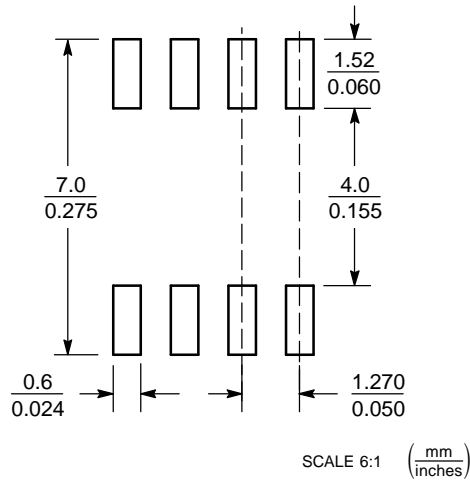


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative